SCREEN IR Day 2025

Investor Relations
Corporate Communications Department
SCREEN Holdings Co., Ltd.

Cautionary statements:

- The earnings forecasts, contained in these materials and communicated verbally, are made in accordance with currently available information and rational assumptions. SCREEN Holdings does not promise that the forecasts or estimates will be accurate. Therefore, it should be noted that actual results could differ significantly due to a variety of factors.
- Figures are rounded down to eliminate amounts less than ¥100 million, except per share figures. Ratios are rounded off.
- SCREEN's fiscal year (FY) covers the period from April 1 to March 31 of the following calendar year. (e.g. FY2026/03 = April 1, 2025 – March 31, 2026)

Agenda

- **SCREEN Group's growth strategy** ..... 20 min
- **Q&A session** ..... 25 min

---------- *Intermission (10 min)* ----------

- **SPE wet etching and cleaning trends** ..... 20 min
- **Advanced packaging trends and outlook** ..... 15 min
- **Q&A session** ..... 25 min

For in-person participants only:

- **IIC Tokyo tour** ..... 30 min
- **Social gathering** ..... 60 min

Introduction of our CEO

Masato Goto

Representative Director, President and CEO
SCREEN Holdings Co., Ltd.

Place of birth: Tokyo

Hobbies: Camping, kayaking, smoke cooking

1990	Joined Dainippon Screen Mfg. Co., Ltd. (now SCREEN Holdings)
1995	Seconded to DAINIPPON SCREEN ENGINEERING OF AMERICA, LLC.
2001	Seconded to DAINIPPON SCREEN (DEUTSCHLAND) GmbH
2009	Head of Production, Semiconductor Equipment Company
2011	Vice President, Semiconductor Equipment Company
2014	Director, SCREEN Semiconductor Solutions Co., Ltd.
2019	Representative Director and President, SCREEN Semiconductor Solutions Co., Ltd.
2024	Senior Managing Executive Officer, Head of Corporate Strategy, SCREEN Holdings Co., Ltd.
2025	Representative Director, President and CEO, SCREEN Holdings Co., Ltd.

SCREEN Group's growth strategy

SCREEN Holdings Co., Ltd.

Masato Goto
Representative Director,
President & CEO

Paving the way for SCREEN's future growth

Corporate Philosophy

Purpose

Innovation for a Sustainable World

Sharing the Future	Building a better future for society with commitment and integrity
Personal Development	Realizing everyone's full potential through trust and teamwork
The Pursuit of Technological Excellence	Exploring technologies while integrating with innovative collaboration

Founder's Motto

Shi Ko Ten Kai Broadening everyone's thoughts and horizons for innovation

Building a world that truly values humans

Nothing can replace real communication that connects people. That is why human–technology synergy is increasingly important.

The SCREEN Group is engaged in multiple, diverse businesses, including our mainstay SPE business and original printing-related business, but a common thread connecting all of them is the capability to contribute to the development of communication tools through technology.

This, I firmly believe, is where our corporate purpose lies. By providing solutions from multiple angles through our business activities, and connecting humans and technology, we aim to become indispensable to society.

SCREEN at a glance

Year founded

1868

Year established

1943

Net sales

¥625.2 bn

Operating margin

21.7%

FY2025/03

Market capitalization

as of November 30, 2025

¥1,226.1 bn

Group employees

6,415

Credit rating*

A+

Outlook: Stable

* Long-term issuer rating by the Japan Credit Rating Agency, Ltd. (JCR)

2024 market share*

SPE	No. 1 global share	Single wafer cleaning equipment
	No. 1 global share	Batch-type cleaning equipment
	No. 1 global share	Spin scrubbers
GA	No. 1 global share	POD equipment (roll-fed inkjet printing)
	Top-class global share	CTP equipment
FT	No. 1 global share	Coater/developers
PE	Top-class global share	Direct imaging systems for solder resists

* Market shares are based on equipment category totals, including data from SCREEN, in a calendar year basis.

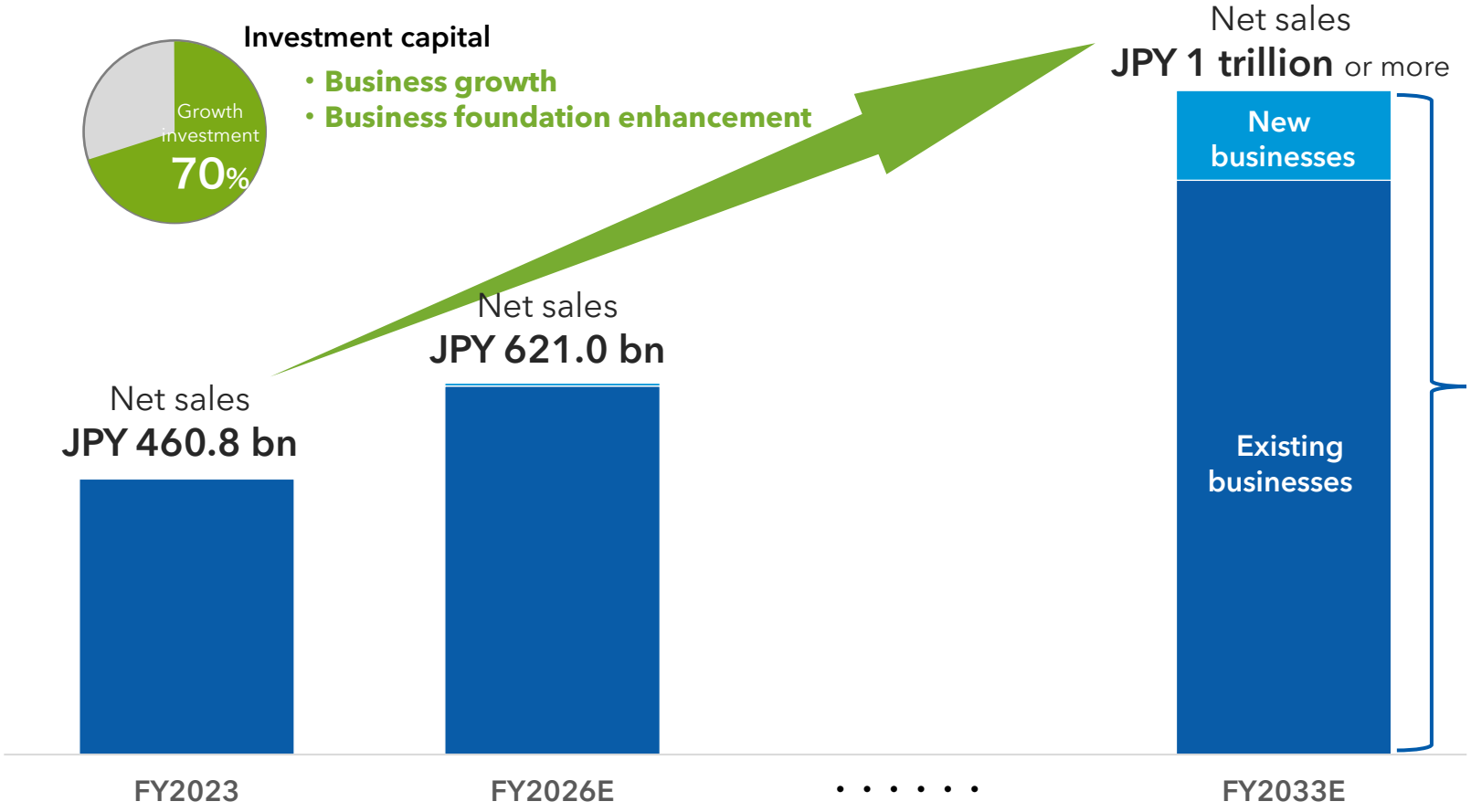
Agenda

- **10-year vision and roadmap**
- **Value Up Further 2026**
  - **Cash allocation**
    a. Growth investment
    b. Our new R&D center
  - **Shareholder returns**
  - **Business growth strategy**
    a. Portfolio management
    b. Core technologies redefined
    c. Progress toward the 3-yr financial targets
    d. New business and innovation management
- **Summary**

Financial & non-financial targets in the Management Grand Design

10-year vision for enhancing corporate value

Basic policy: To grow our existing businesses and create new businesses, 70% of our investment fund* will be allocated to growth, with the aim of achieving the Management Grand Design's FY2033/03 targets of net sales of ¥1 trillion or more and an operating margin of 20% or above.



Further growth in semiconductor-related fields

- Maintain the current revenue share of the existing SPE business
- Expand semiconductor-related sales in advanced packaging

Higher overall revenue share

*Operating cash flow before research expenses

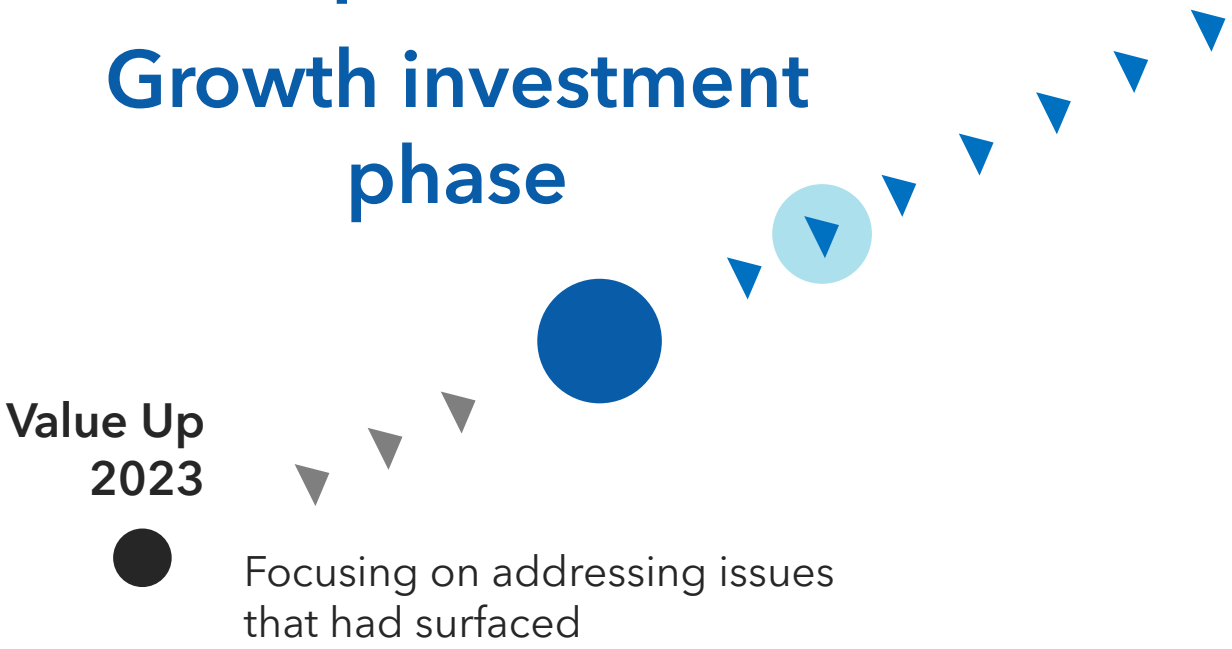
Moving to the growth investment phase:
a step beyond existing business growth

Value Up Further 2026

Growth investment phase

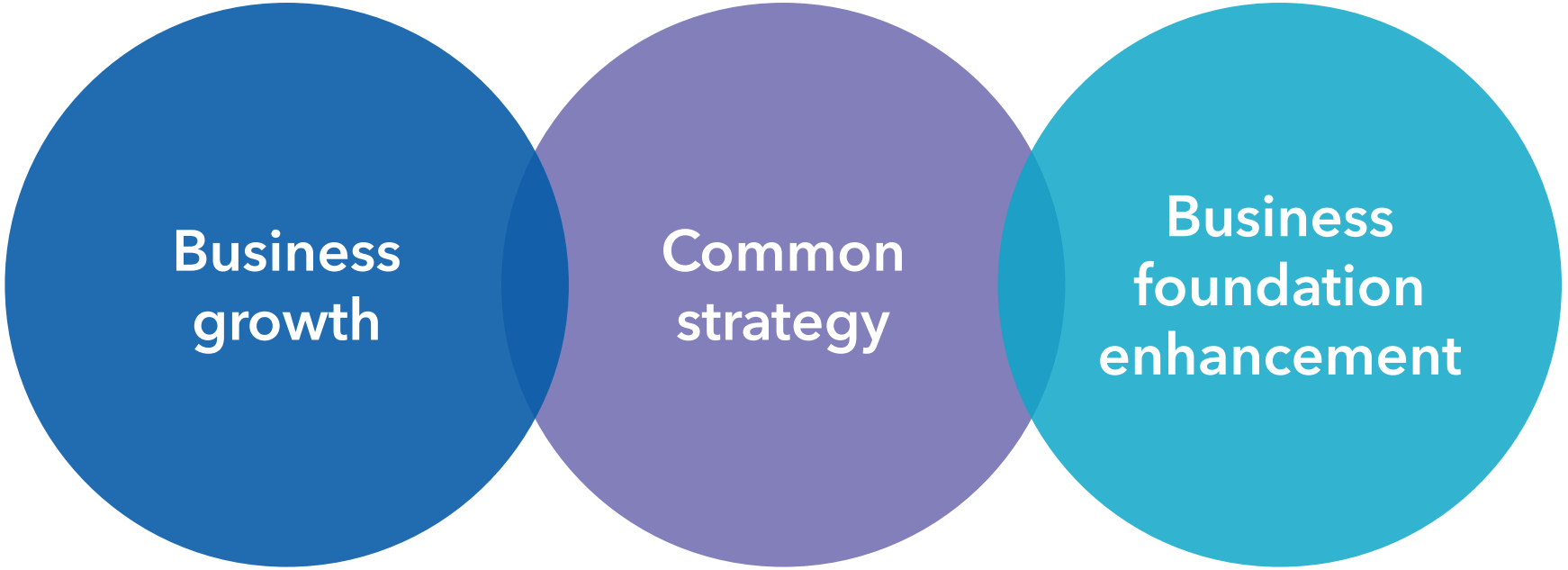
2032

JPY 1 trillion in net sales

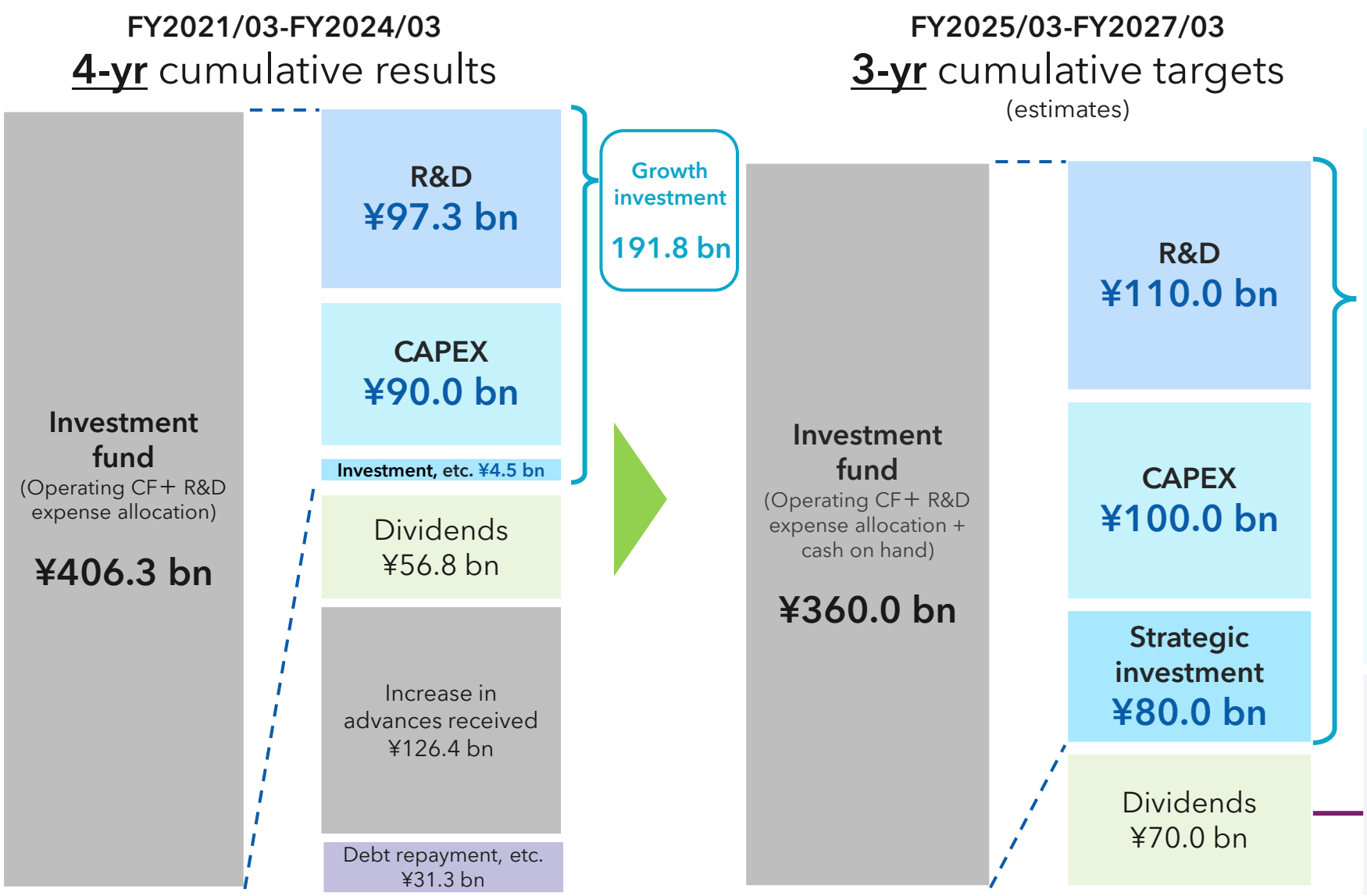


Paving a solid path for growth

While maintaining the high profitability and efficiency achieved under Value Up 2023, we are dedicating the current three-year phase to **building a foundation for sustainable growth**.



Value Up Further 2026: Cash allocation (3-yr cumulative)

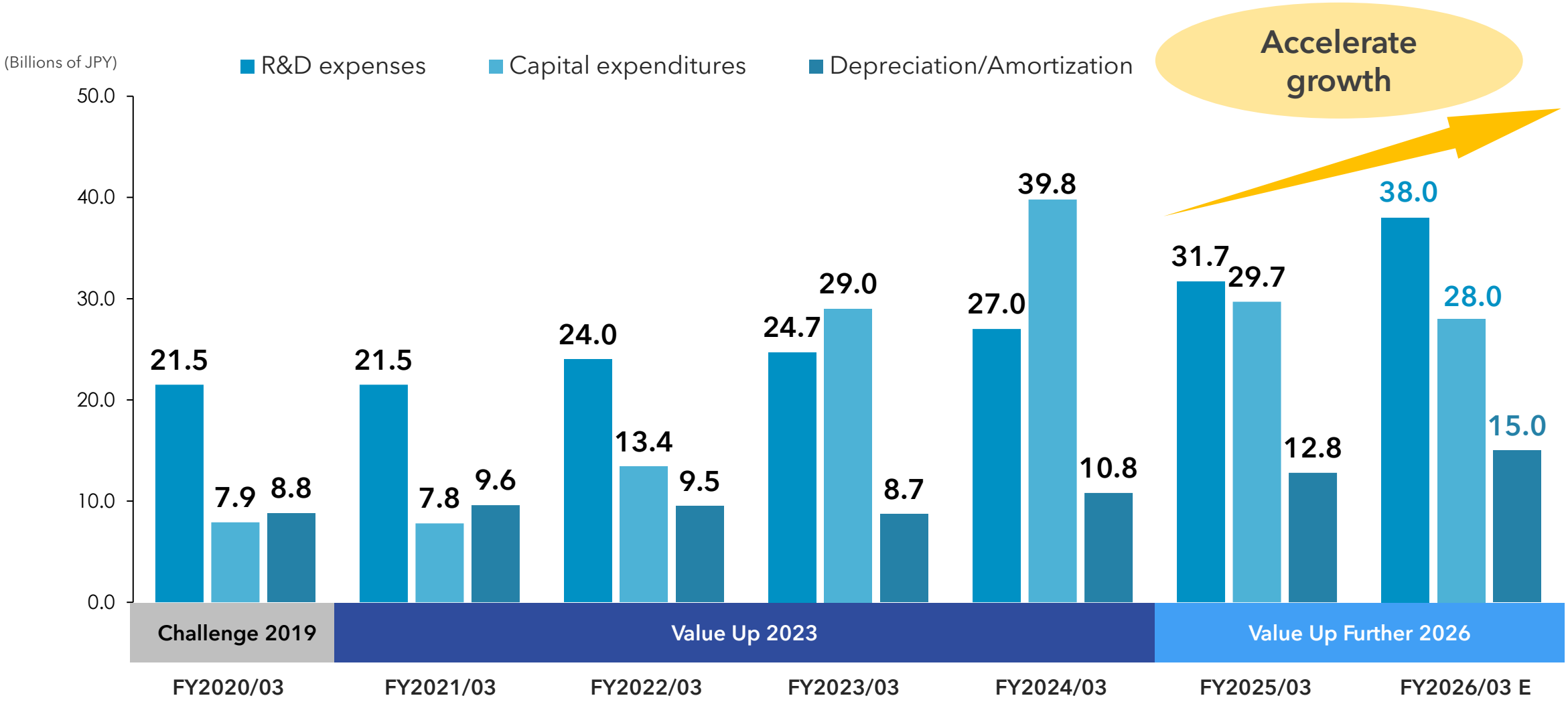


Focused allocation on growth investment

- Allocating approx. 80% (¥290bn) of investment fund to growth investment, reaping the benefits in the next 3-yr phase
- Reinforcing the business foundation toward achieving ¥1tn net sales in FY2032
- Accelerating business growth combining organic growth with strategic investment such as M&A

- Maintaining a dividend payout ratio of 30% or above
- Share buybacks to be considered depending on cash flows and the progress in growth investment

Value Up Further 2026: Growth investment



Value Up Further 2026: Strategic investment

1 Accelerate the growth of advanced packaging business

- **Development of Cu-Cu low-temperature hybrid bonding**
  Acquisition of an R&D business in wafer bonding from Nikon
- **Expanding product portfolio for PLP coaters and direct imaging systems**

2 Advance the development of world-leading wet clean technology Enhance product competitiveness in SPE

ATCA, an overseas R&D center for semiconductor manufacturing processes to be established in Albany, New York

- Acquired land in Yasu City, Shiga
- Acquired production site and building in Nagaokakyo City, Kyoto Prefecture
- Life Sciences: Acquired shares of Kyo Diagnostics and made it a subsidiary
- GA: Acquired Germany-based CGS as a group company

Our new R&D center

Overview of ATCA

- **Objective**

  To i) accelerate elemental technology validation and equipment development for our global SPE business, and to ii) shorten the time required for elemental technology validation by conducting leading-edge device characterization on site.

- **R&D facility**

  ATCA will be located within Albany NanoTech Complex, the state-of-the-art semiconductor facility operated by NY Creates (NYCR).

  It will be using NYCR's clean room and other infrastructure to pursue solo research as well as joint research with global partners.

› We will aim to increase our presence in wet cleans as well as thermal processing and advanced packaging.

Our new R&D center

Overview of ATCA

● Company information

Company name	SCREEN Advanced Technology Center of America, LLC (ATCA)
Location	201 Fuller Road, Suite 306, Albany, NY 12203, U.S.A.
Representative	Ian Brown, PhD, President
Established	December 1, 2025

● Facility information

Floor area	Clean room: 929 m^2 Office space: 462 m^2
Main purpose	R&D for leading semiconductor production processes and equipment
Total investment	Around JPY 12.0 billion expected by March 31, 2027, excluding other expenses

Role of the new R&D center

- Working with IBM to develop leading-edge device processes and conduct device characterization near our clients.
- Serving our clients worldwide by developing new machines featuring our most advanced technologies.

Rakusai @Kyoto

Elemental technology development, including seeds search

PTC @Hikone

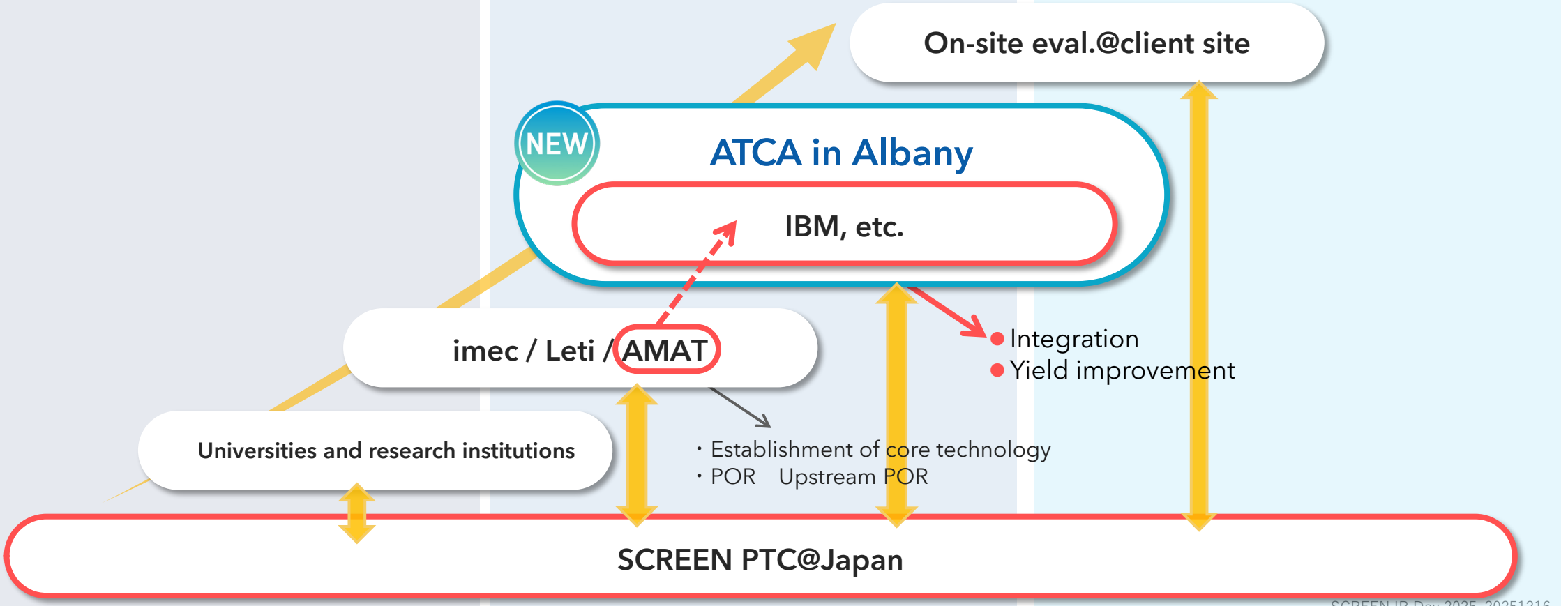
Mechanical development in collaboration with manufacturing and engineering teams

ATCA @Albany

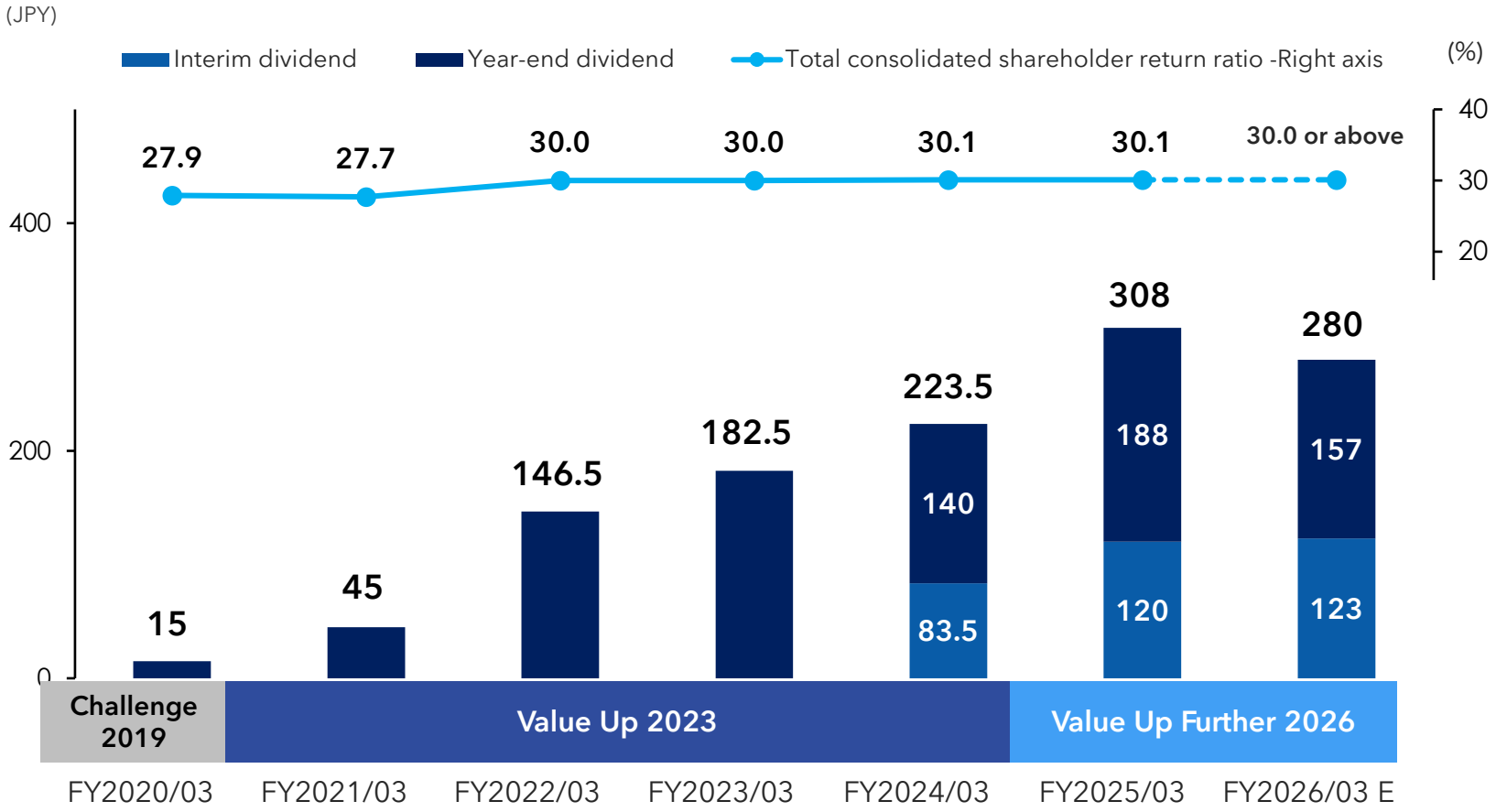
Solo research and joint research projects in collaboration with global partners

Our R&D pipelines

PoC	Prototyping/Integration	Large-scale manufacturing
Basic research and development Adaptation to new materials, new structures, and related technologies	Transition to large-scale production Overcoming the hurdles for large-scale production	Development for large-scale production



Value Up Further 2026: Shareholder returns



Shareholder return policy

Dividend payout ratio: 30% or above

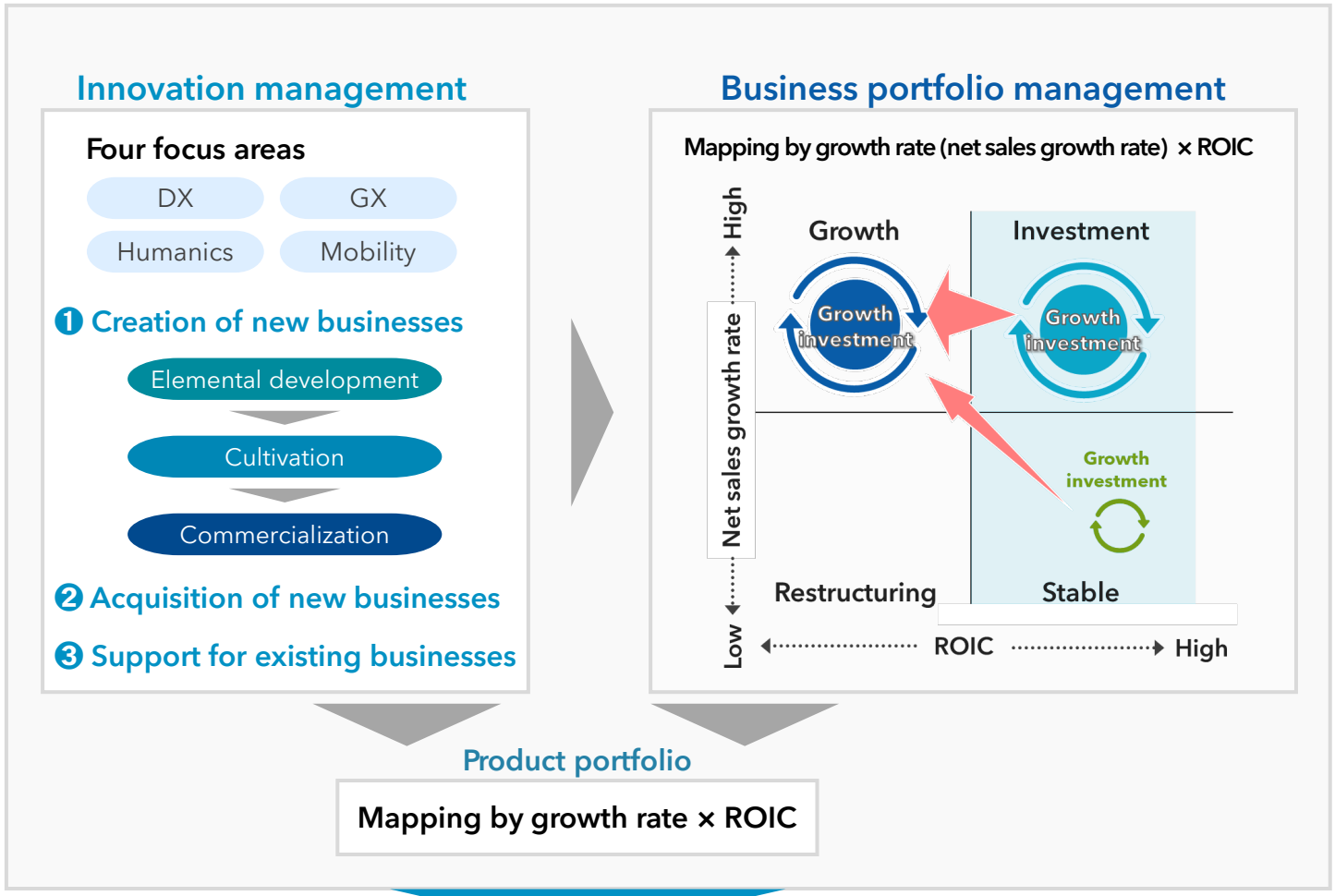
Other shareholder returns

Flexible share buybacks to be implemented depending on cash flows and the progress in growth investment

- **Implemented share buybacks worth approx. ¥30bn in Feb–Apr. 2025**

Note: The Company implemented a stock split of common stock in the ratio of 1 share into 2 shares on October 1, 2023.
The dividend per share is calculated based on the assumption that the stock split was conducted at the beginning of the fiscal year ended March 2020.

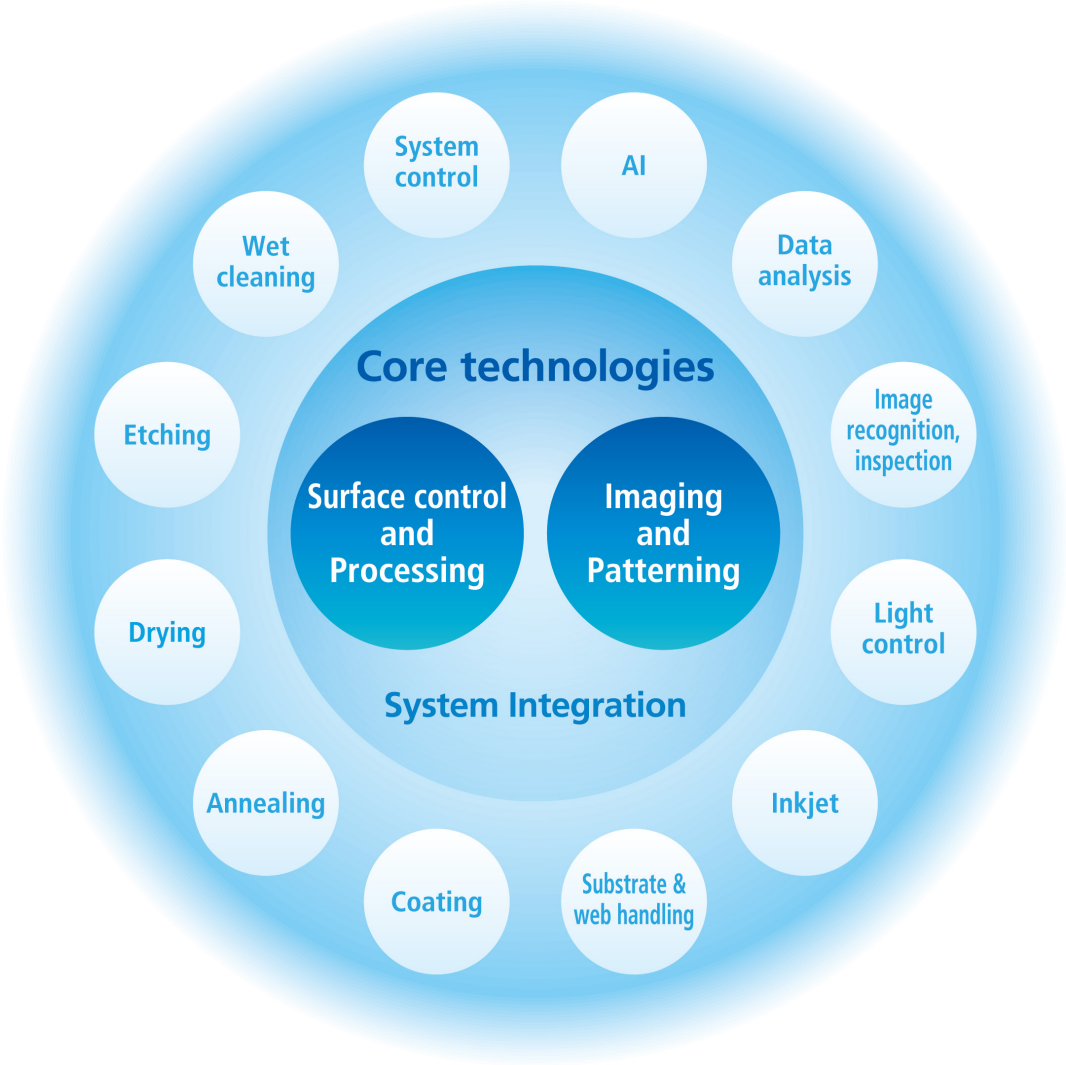
Value Up Further 2026: Portfolio management



- Revisiting the exit criteria applied to existing and new businesses
- Redefining our goals with respect to portfolio management with a forward-looking mindset, considering a variety of options, including M&A

Note: Portfolio management is done under the leadership and supervision of the holding company, with periodical reports made to and confirmed by the HD Board of Directors.

Core technologies redefined



Redefined our core technologies in line with the revised corporate philosophy

Core technologies:

Surface control and processing and **imaging and patterning**, combined through **system integration**

Elemental technologies:

Basic technologies derived from the core technologies are positioned around them like satellites

Value Up Further 2026: Progress toward the 3-yr financial targets

		Value Up Further 2026 (FY2025/03-FY2027/03) 3-yr cumulative targets	1st year results (FY2025/03)	2nd year forecasts (FY2026/03)	2-year cumulative forecasts
Consolidated	Cumulative sales	**¥1.8 trillion** or more	¥625.2 bn	¥621.0 bn	¥1,246.2 bn
	Average OP margin	19% or above	21.7%	18.8%	20.3%
	ROIC	15% or above	24.7%	19.6%	-
	Shareholder Returns	Consolidated dividend payout ratio:30% or above (Flexible share buybacks will be implemented depending on the progress of growth investment)	• Consolidated dividend payout ratio: 30.1% • Implemented share buybacks	Consolidated dividend payout ratio:30% or above (Flexible share buybacks will be implemented depending on the progress of growth investment)	Consolidated dividend payout ratio:30% or above (Flexible share buybacks will be implemented depending on the progress of growth investment)
SPE	Cumulative sales	**¥1,500.0 bn** or more	¥519.5 bn	¥502.0 bn	¥1,021.5 bn
	Average OP margin	23–25%	26.4%	24.1%	25.3%
GA	Cumulative sales	**¥150.0 bn** or more	¥53.0 bn	¥53.0 bn	¥106.0 bn
	Average OP margin	6–9%	8.1%	4.7%	6.4%
FT	Cumulative sales	**¥100.0 bn** or more	¥35.8 bn	¥45.5 bn	¥81.8 bn
	Average OP margin	3–5%	8.5%	17.4%	13.5%
PE	Cumulative sales	**¥50.0 bn** or more	¥14.1 bn	¥15.0 bn	¥29.1bn
	Average OP margin	12–15%	7.5%	6.7%	7.1%

Note: The above figures are predicated on organic growth.

Value Up Further 2026: Business growth strategy

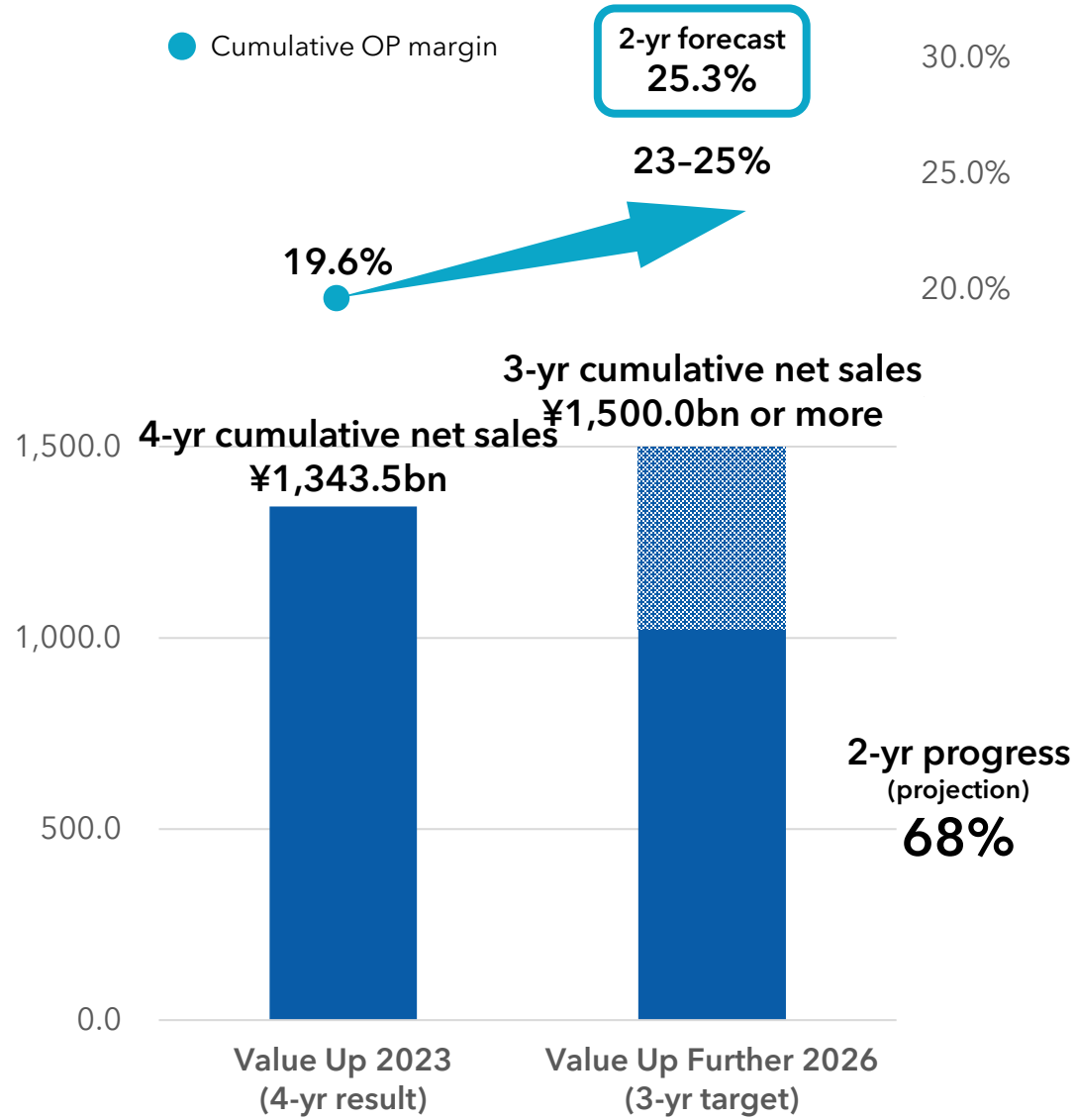
SPE

Main initiatives

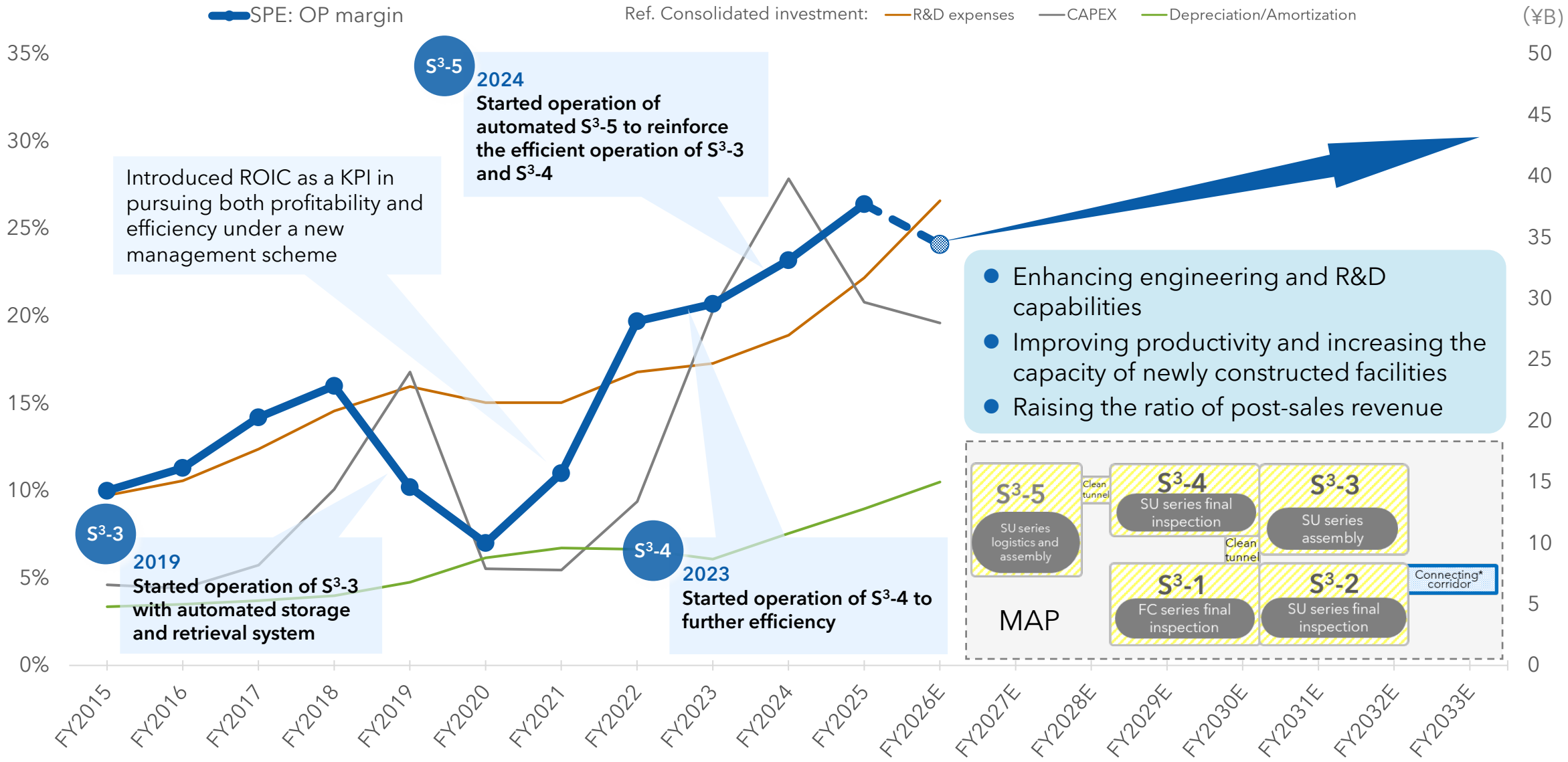
1. Improve the market share of the cleaning equipment
   >> ***Develop an optimal R&D environment*** and ***win new PoRs***
2. Expand the production capacity
   >> Shorten the lead time by improving productivity, pursue automation
3. Enhance the business foundation
   >> Streamline operation through DX
   >> Recruit & nurture top talents

3-yr cumulative targets

Net sales	OP margin
¥1,500 bn or more	23% – 25%



Improving SPE profitability



Value Up Further 2026: Business growth strategy

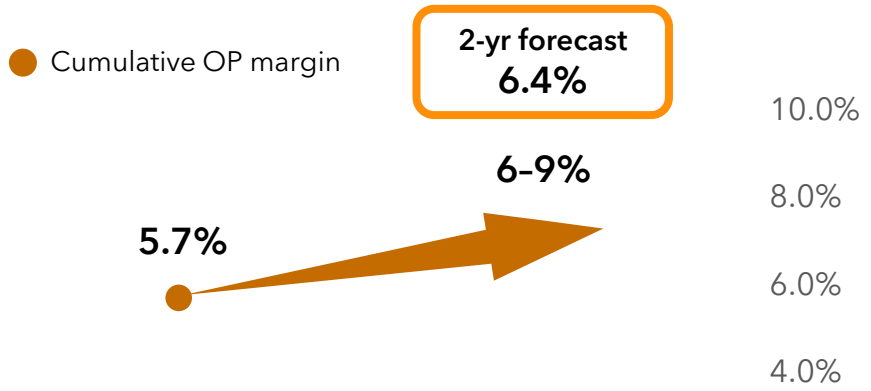
GA

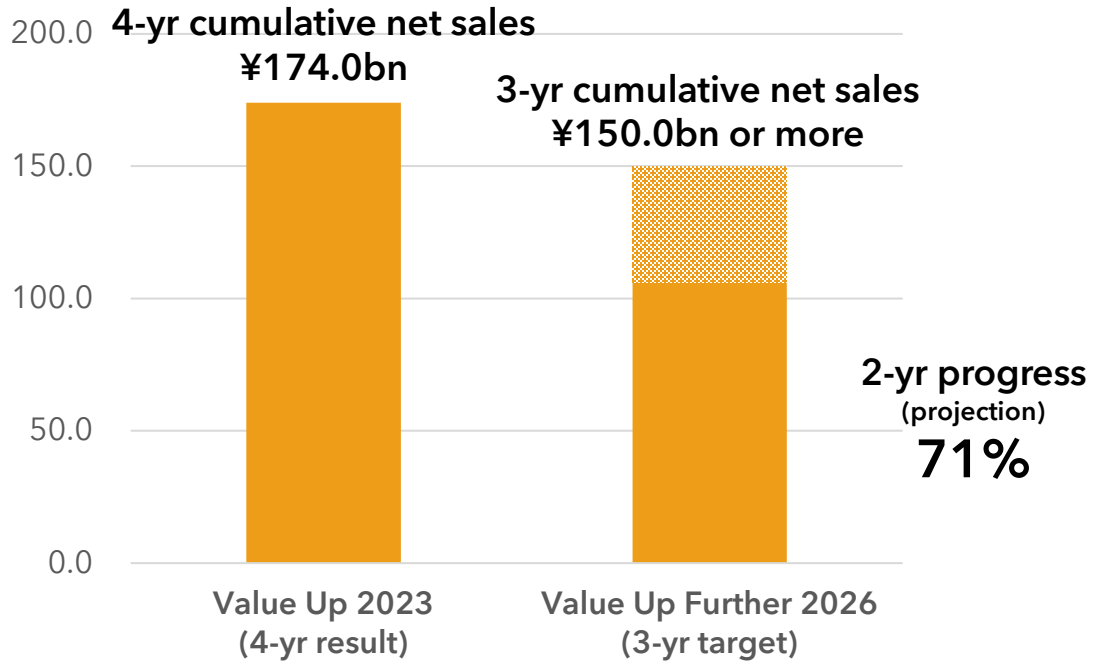
Main initiatives

1. Expand the sales pipelines of POD equipment
   >> Enhance our approach to large-order clients
2. Expand recurring business
   >> Initiatives to improve the operation rate on the client side
3. Establish package printing business

3-yr cumulative targets

Net sales	OP margin
¥150 bn or more	6% – 9%





Value Up Further 2026: Business growth strategy

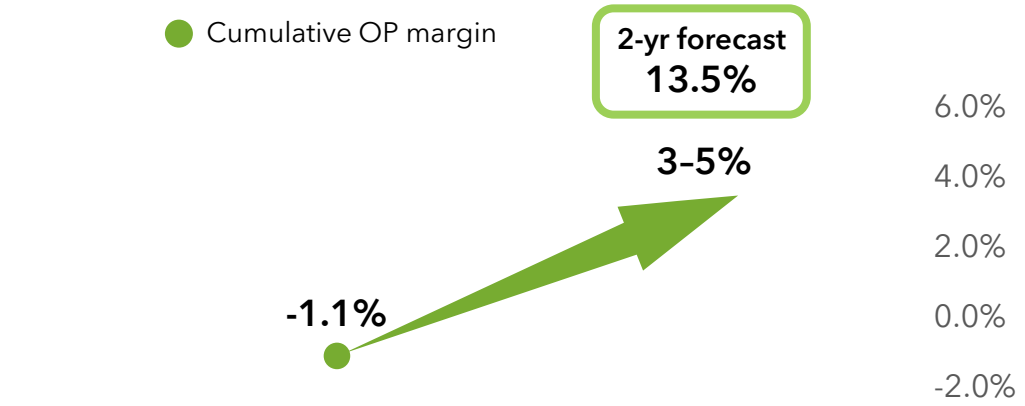
FT

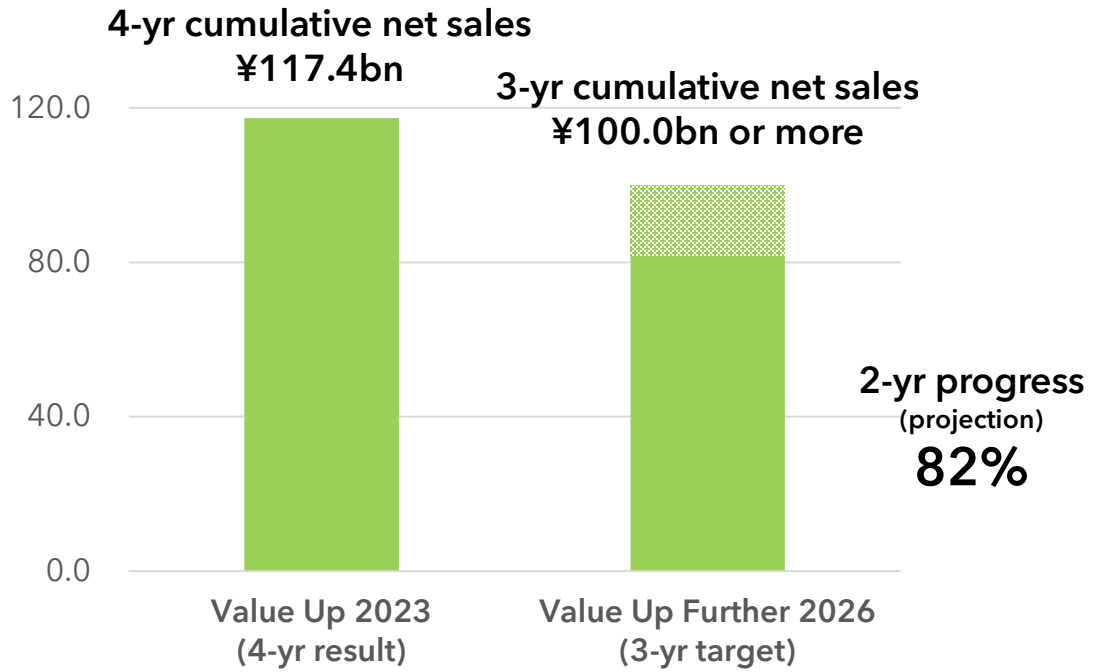
Main initiatives

1. Improve the profitability of display business
2. Enhance our proprietary coating technique and expand the scope of its application
   >> Enhance roll-to-roll products and technologies
3. Expand the scope of internal OEM business
   >> ADPKG and hydrogen-related products

3-yr cumulative targets

Net sales	OP margin
¥100 bn or more	3% – 5%





Value Up Further 2026: Business growth strategy

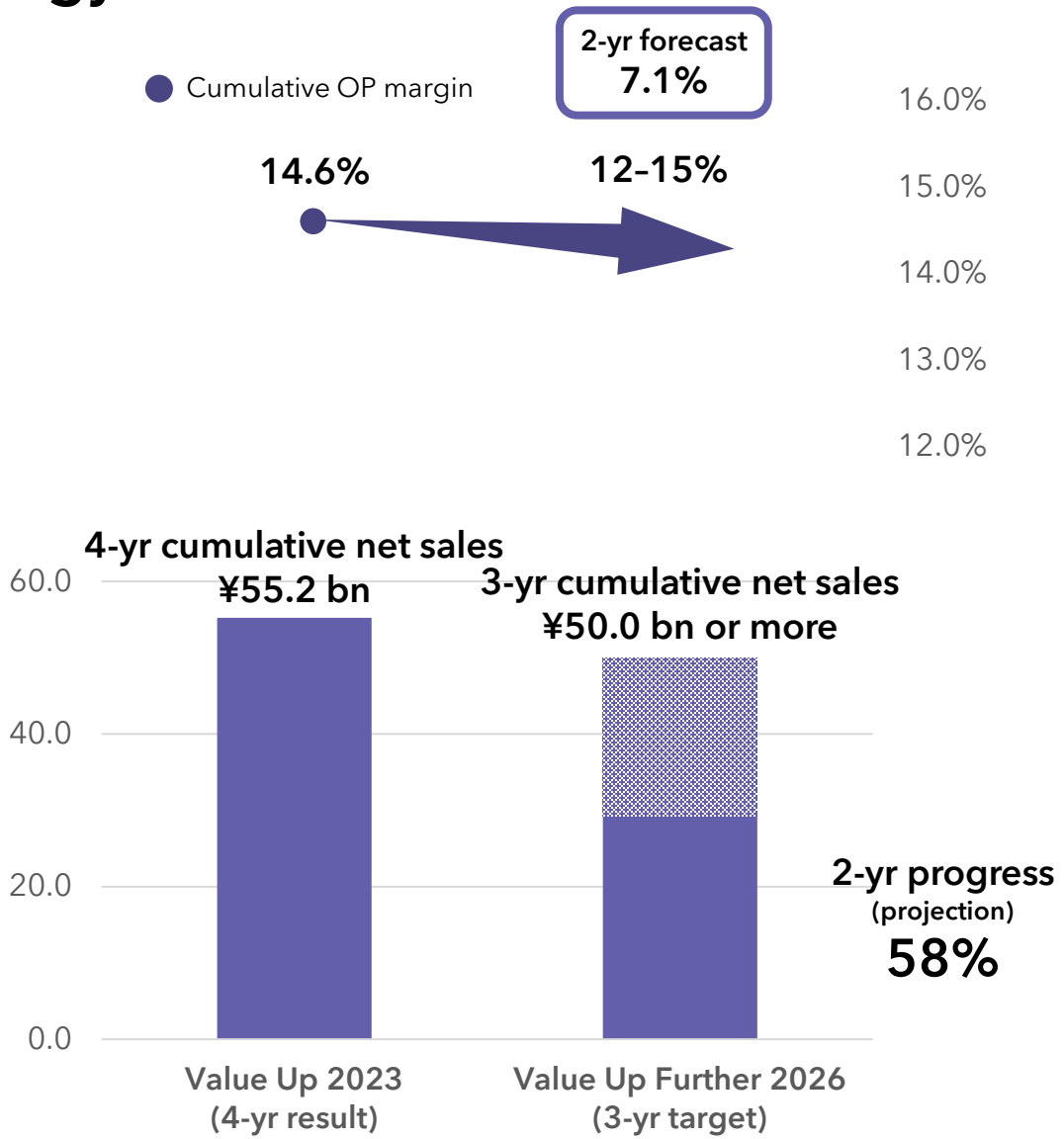
PE

Main initiatives

1. Enhance the presence of the direct patterning equipment in the industry
   >> Increase our market share in direct lithography for solder resists (SR)
   >> Launch direct patterning solutions for circuit pattern resists
2. Expand the use of direct patterning for different applications

3-yr cumulative targets

Net sales	OP margin
¥50 bn or more	12% – 15%



Business growth strategy: New business and innovation management

Creating new businesses that could eventually reach the level of our existing businesses as well as solutions that strengthen the existing businesses, focusing on the four areas based on megatrends we have identified.

Focus areas

DX
Contribute to DX in society
DX in equipment

GX
Contribute to decarbonization
Make low-energy equipment

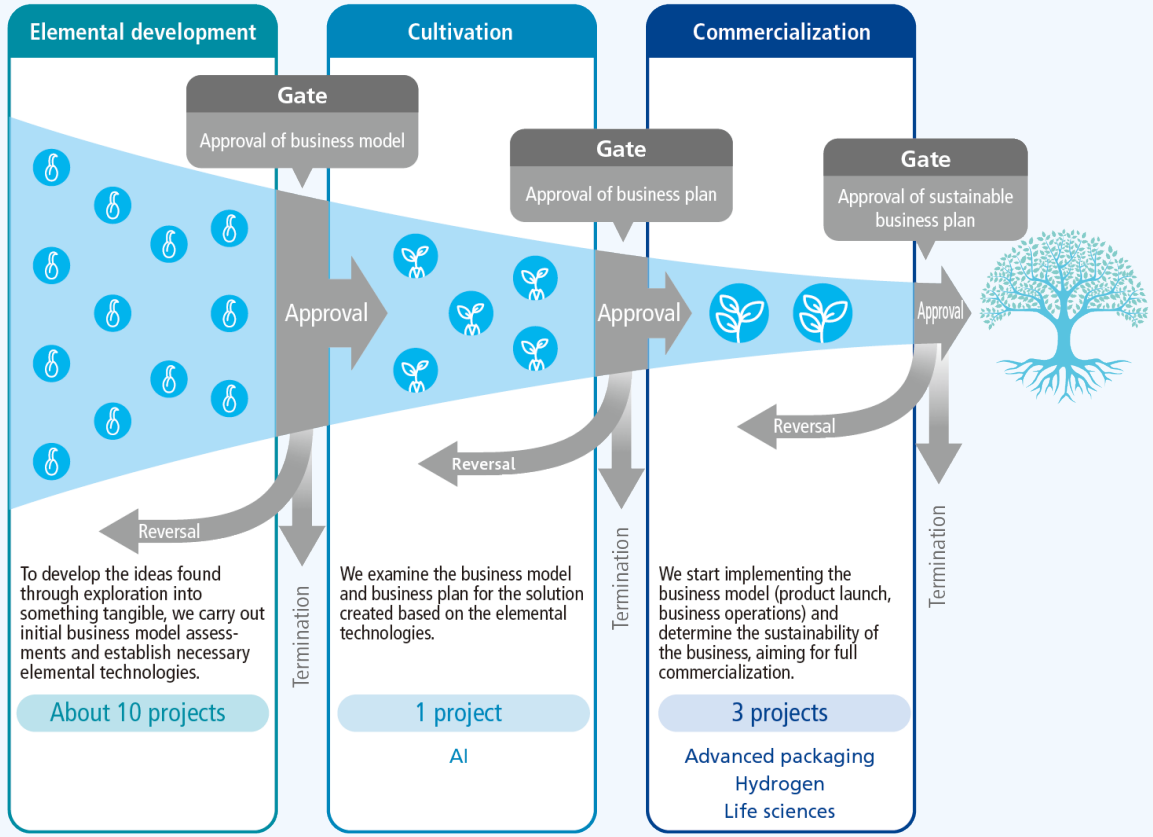
Humanics
Automation/ self-driving
Integrate people and technologies

Mobility
Technologies that support convenient transportation of people and goods

Exploration

① Creation of new businesses

We seek to create solutions with the potential to become new businesses and contribute to the growth envisioned in the Management Grand Design.



② Acquisition of new businesses

We seek to capture opportunities for collaboration with other companies (including investment, M&A, and other forms of capitalization), aiming to create new businesses and expand the existing business portfolio.
Priority investment areas ➡ SPE, advanced packaging, hydrogen energy, etc.

Main results of initiatives in the fiscal year ended March 31, 2025

- Added Kyo Diagnostics K.K., which develops next-generation cancer diagnostic support systems and services, to the Group as a subsidiary
- Added CGS ORIS GmbH, which develops and sells color technology products, to the Group

③ Support for existing businesses

We create solutions that strengthen the existing businesses over the long term.

Value Up Further 2026: Business growth strategy

New Business

Advanced packaging

- Increase the market presence of existing products (direct imaging, coaters)
- Launch new products (Cu-Cu low-temperature hybrid bonding, etc.)
- Become profitable in the final year

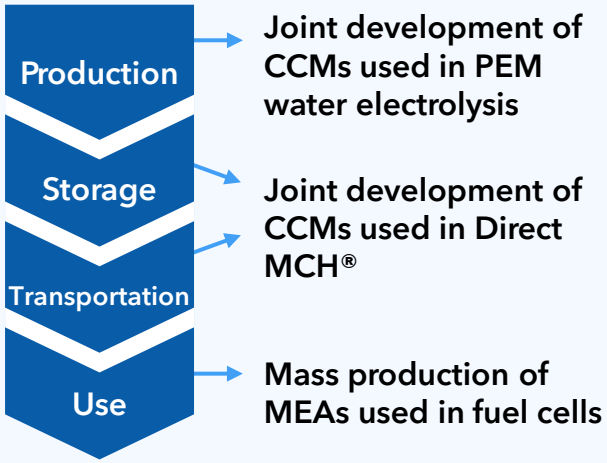
Main initiatives

- **Direct imaging system:** LeVina
- **Coater for panels:** Lemotia
- **Low temperature hybrid bonding machine**

Hydrogen-related business

- Establish an OEM manufacturing framework for hydrogen MEAs
- Become profitable in the final year

Main initiatives



Life sciences

- Expand the sales channels of existing product
  ➡Reinforce cell inspection business
  ➡Step up sales of tablet inkjet printing equipment
- Establish a business model for personalized cancer treatment
- Promoting collaboration for Adriakaim to obtain medical certification

Main initiatives

- **Biosciences:** Cell inspection systems, etc.
- **Pharmaceuticals:** Tablet inkjet printing systems, etc.
- **Medical devices:** Medical devices for organ transplantation

Summary

1. Business portfolio is our top management priority

Realigning our business portfolio to gear it toward further growth, with emphasis on **growth potential** and **efficiency**

2. Allocating investment funds with focus on the growth areas

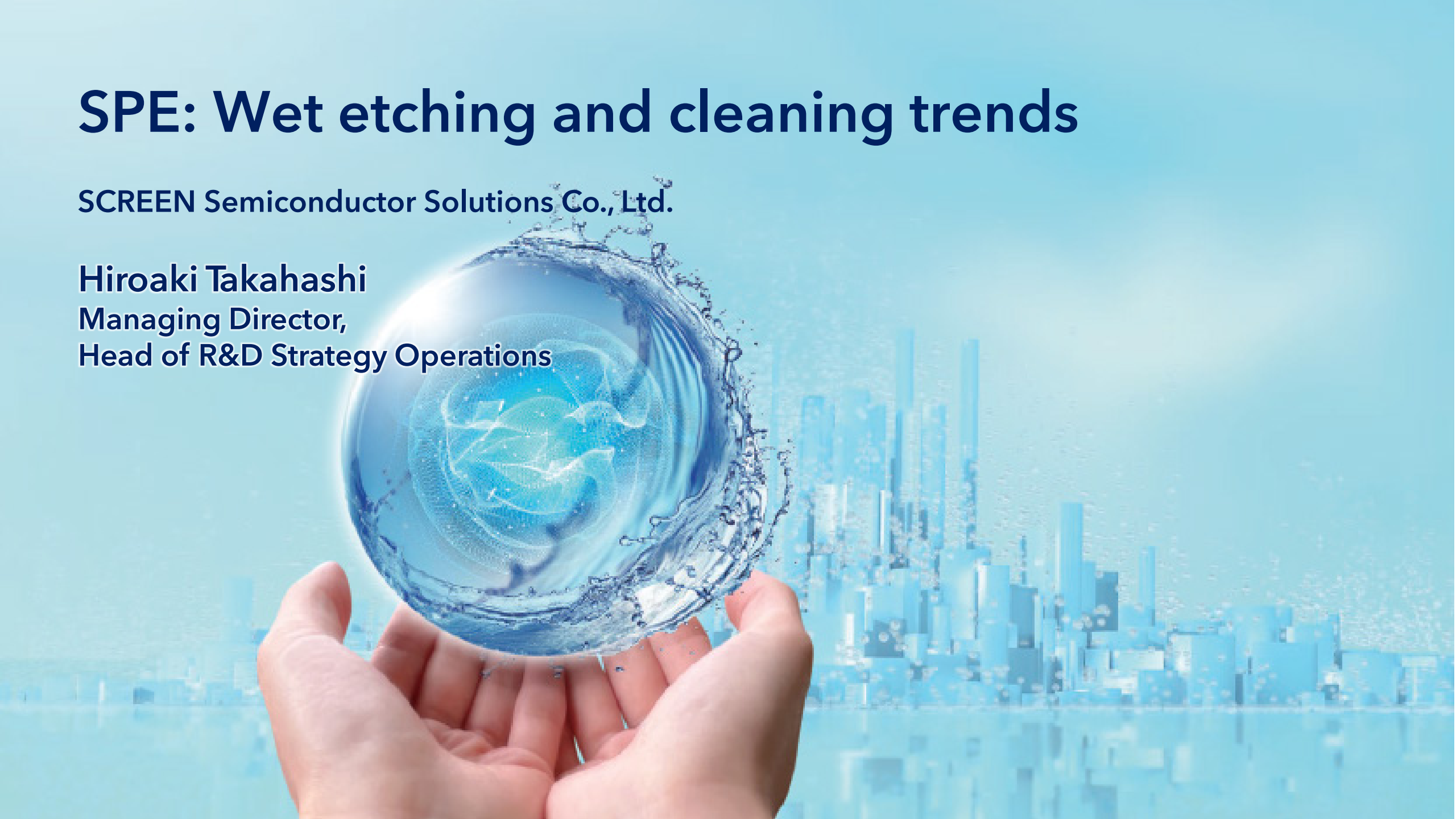
3. Our R&D, engineering, production, and marketing teams will continue to work together to further improve profitability

Committed to showing our stakeholders a solid track record of growth to maximize shareholder returns.

SPE: Wet etching and cleaning trends

SCREEN Semiconductor Solutions Co., Ltd.

Hiroaki Takahashi
Managing Director,
Head of R&D Strategy Operations



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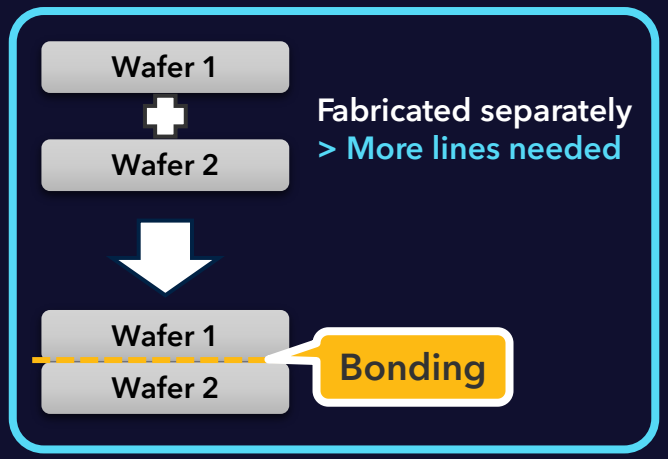
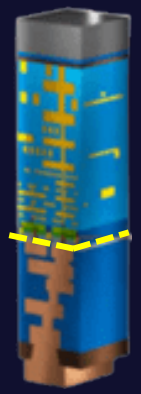
Scaling x 3D integration

BSPDN: Back Side Power Delivery Network
CAR: Chemical Amplifier Resist
CFET: Complementary Field Effect Transistor
MOR: Metal Oxide Resist

"Miniaturization + **Bonding**" is becoming the mainstream in line with the evolving device architecture.

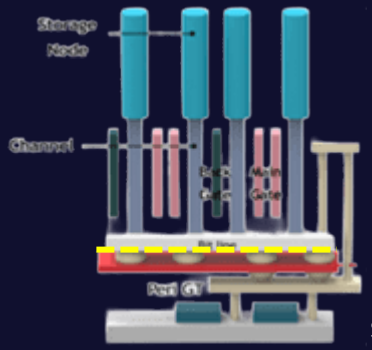


Logic BSPDN



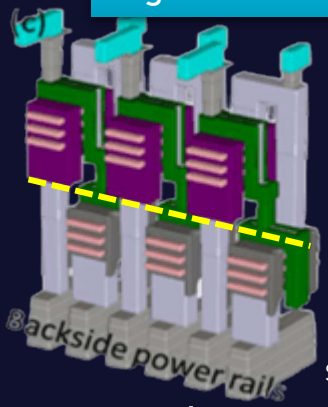
Source: intel, VLSI 2023

DRAM 4F2 VCT



Source: SK hynix, VLSI2024

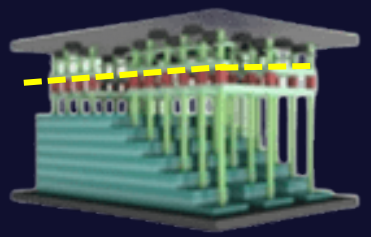
Logic Nanostack



Source: IBM, VLSI2025

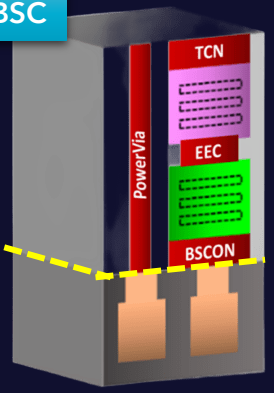
CY2018 — CY2026 — CY2027 — CY2028 — CY2029 — CY2030 — CY2031

3D-NAND



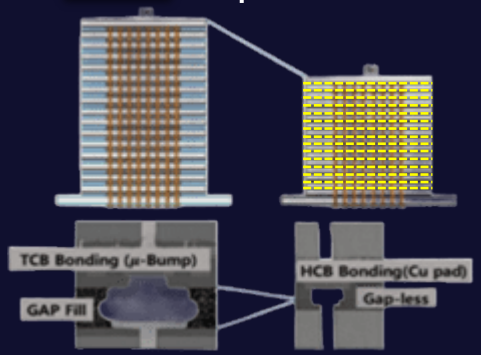
Source: YMTC, FMS 2018

Logic BSC



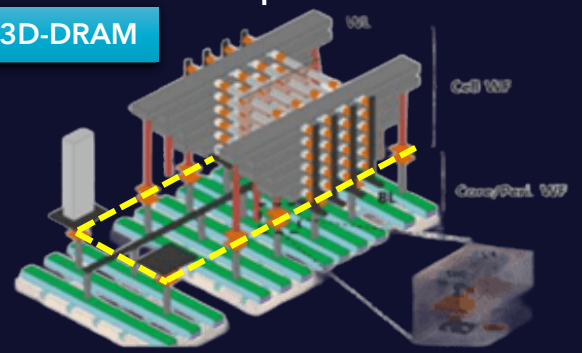
Source: M. Kobrinsky IEDM 2024

HBM



Source: Samsung, ECTC2024

3D-DRAM



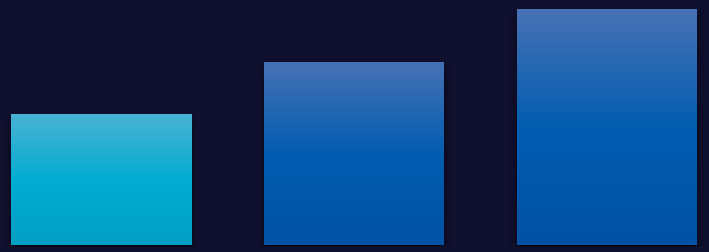
Source: Samsung, VLSI 2023

Expected increase in device processing steps, by structure

(SCREEN's estimates)

Logic

- **Transistor structure: FF > NS > CFET**
- **Back-side wiring through bonding: Post-A16**
- **Transistor formation through bonding: sCFET**



FF: FinFET
NS: Nanosheet
sCFET: sequential Complementary Field-Effect Transistor

DRAM

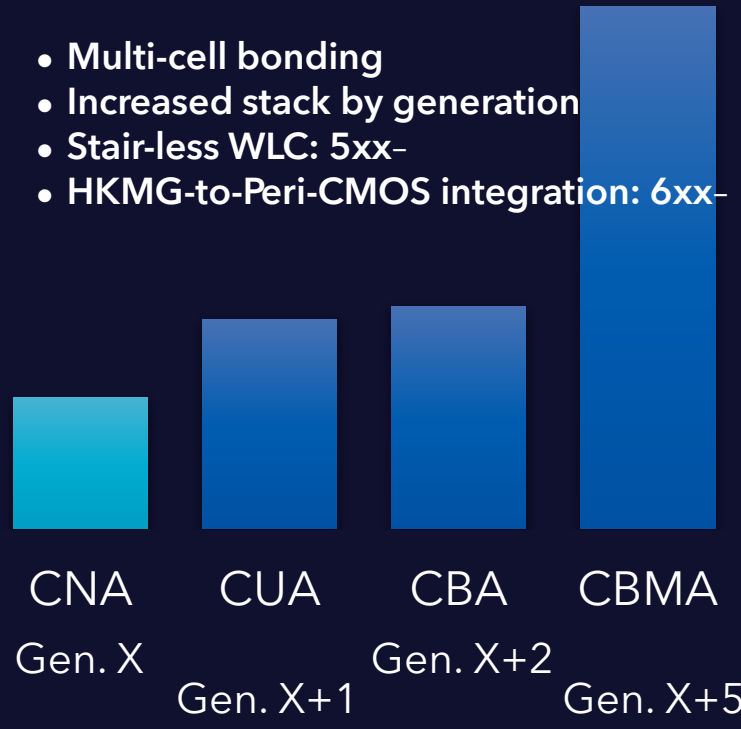
- **Memory cell structure: 6F2 > 4F2**
- **CMOS/Memory cell bonding: 4F2**

VCT: Vertical Channel Transistor

*3D-DRAM under examination

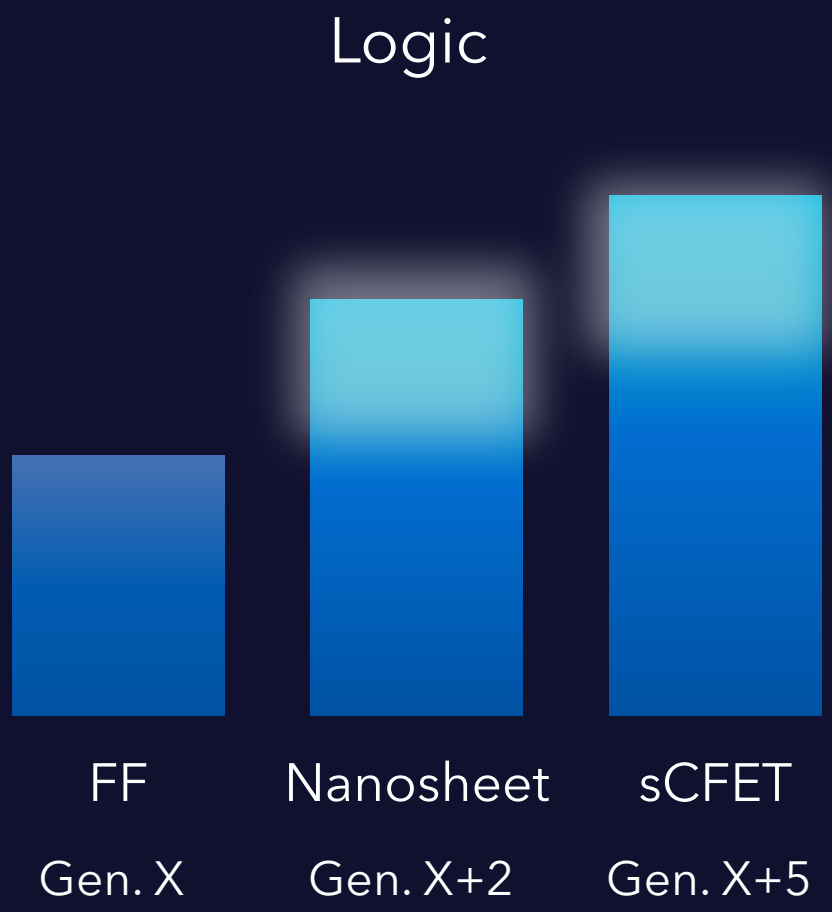
NAND

- **Multi-cell bonding**
- **Increased stack by generation**
- **Stair-less WLC: 5xx–**
- **HKMG-to-Peri-CMOS integration: 6xx–**



CNA: CMOS Near to Array
CUA: CMOS Under Array
CBA: CMOS Bonded to Array
CBMA: CMOS Bonded to Multi-Array

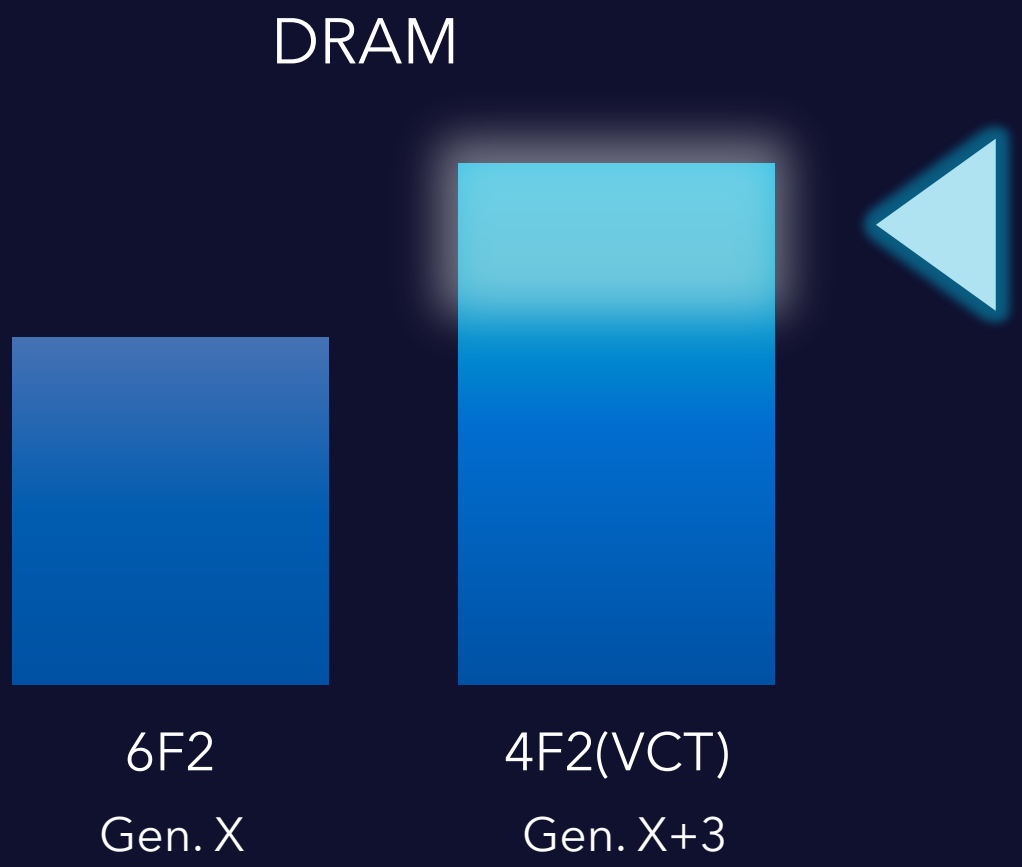
Expected increase in SCREEN SPE's sales: Logic



Brushing up wet clean technology to accommodate the leading-edge structure and materials

FF: FinFET
sCFET: sequential Complementary Field-Effect Transistor

Expected increase in SCREEN SPE's sales: DRAM



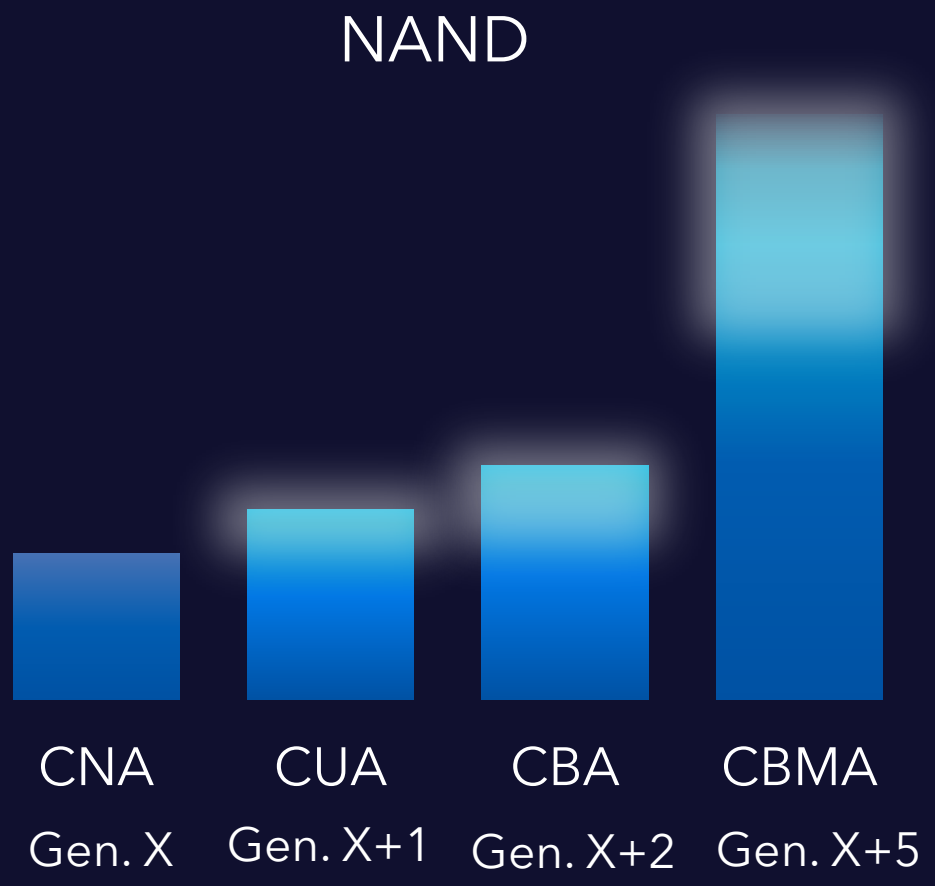
Expanding cleaning opportunities with Logic technology introduced in DRAM, and 3D packaging

Boosting market share by winning new PORs in DRAM by leveraging our Logic expertise

VCT: Vertical Channel Transistor

*3D-DRAM under examination

Expected increase in SCREEN SPE's sales: NAND



CNA: CMOS Near to Array
CUA: CMOS Under Array
CBA: CMOS Bonded to Array
CBMA: CMOS Bonded to Multi-Array

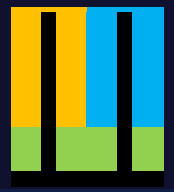
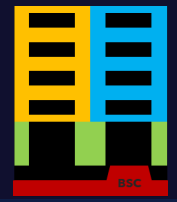
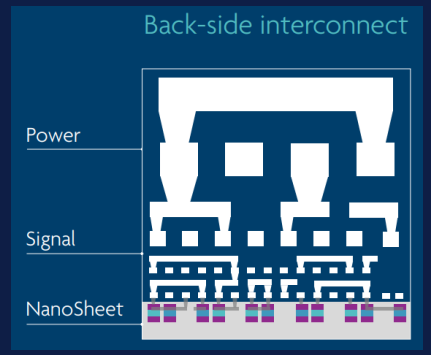
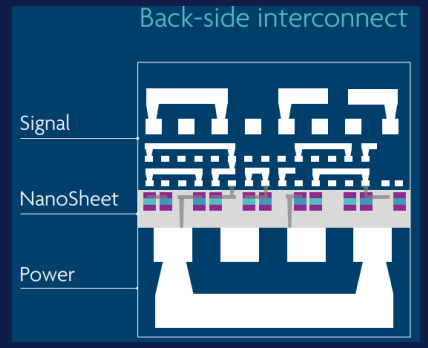
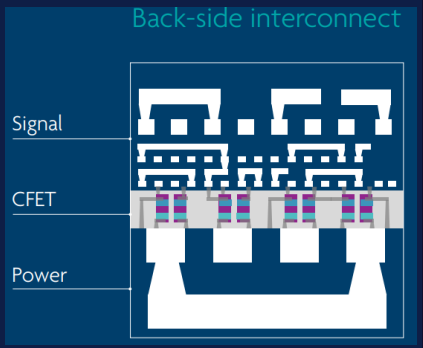
Expanding cleaning opportunities with Logic technology introduced in NAND, and 3D packaging

Process switch from batch cleaning to single-wafer cleaning with HKMG integration

Boosting market share by winning new PORs in NAND by leveraging our Logic expertise

Logic roadmap

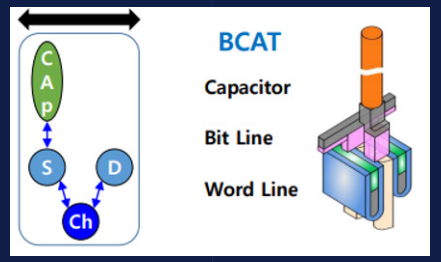
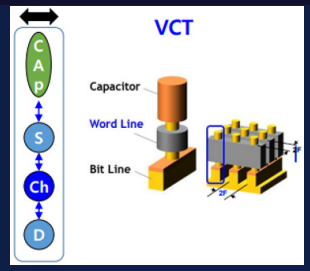
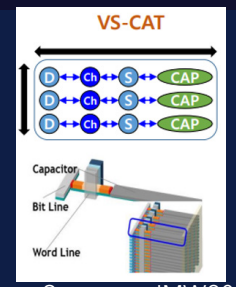
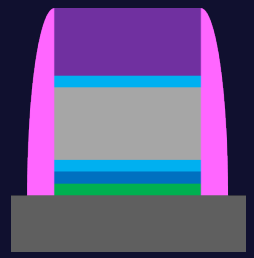
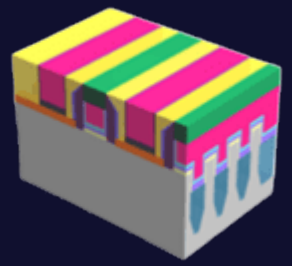
BSPDN: Back Side Power Delivery Network
CAR: Chemical Amplifier Resist
CFET: Complementary Field Effect Transistor
MOR: Metal Oxide Resist

CY	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032
HVM Gen.	N3		N2			A16/A14		A10		A7	
Transistor						Scaled 		Extended 			
EUV	NA=0.33				NA=0.33, NA=0.55			NA=0.55			
Resist	CAR		CAR			CAR, MOR		CAR, MOR		CAR, MOR	
Metal pitch [nm]	23nm		22nm			21nm		18nm		17nm	
Minimum defect	11.5nm		11nm			10.5nm		9nm		8.5nm	
BSPDN	imec		 Source: imec, ITF JAPAN 2024			 Source: imec, ITF JAPAN 2024				 Source: imec, ITF JAPAN 2024	

DRAM roadmap

BCAT: Buried Channel Array Transistor
CAR: Chemical Amplifier Resist
CBA: CMOS Bonded to Array
CNA: CMOS Near to Array
HKMG: High-k Metal Gate
MOR: Metal Oxide Resist

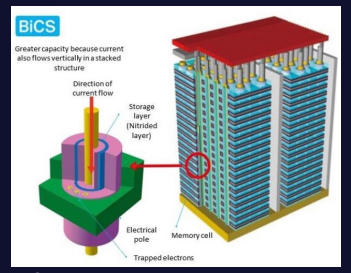
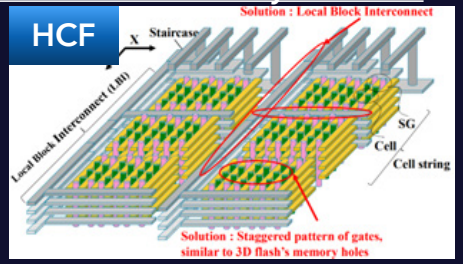
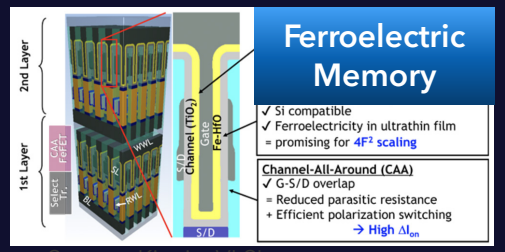
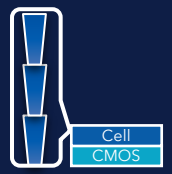
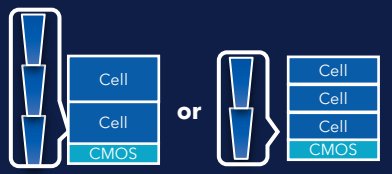
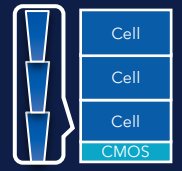
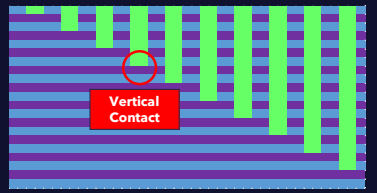
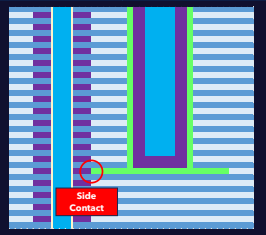
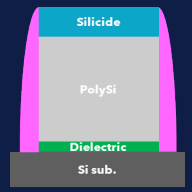
VCT: Vertical Channel Transistor
VS-CAT: Vertically Stacked Cell Array Transistor

CY	23	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033
Gen. (1.5year/cycle)		D1B	D1C		D1D	D0A		D0B	D0C or 3D		D0D or 3D
Cell layout		6F2	6F2		6F2	4F2		4F2	4F2 or 3D		3D
		 Source: Samsung, IMW2024				 Source: Samsung, IMW2024				 Source: Samsung, IMW2024
CMOS layout		CNA Cell CMOS	CNA		CNA	CBA Cell CMOS		CBA	CBA		CBA
EUV		NA=0.33				NA=0.33, NA=0.55 (for Planar) , No process (for 3D-DRAM)					
EUV resist		CAR / MOR	CAR / MOR		CAR / MOR	CAR / MOR		CAR / MOR	CAR / MOR		CAR / MOR
Peri-CMOS		HKMG (Gate First)	HKMG (Gate First)		HKMG (Gate First)	HKMG FinFET		FinFET	FinFET		FinFET
											

Source : SK hynix, VLSI2025

NAND roadmap

CBA: CMOS Bonded to Array
CUA: CMOS Under Array
eWLC: exponential Word Line Contact
HCF: Horizontal Channel Flash
HKMG: High-k Metal Gate
VC: Vertical contact

	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033
Layer	2yy/3xx L		4xx L		6xx L		8xx L		10xx L	
Structure	 Source: Kioxia				**Alternative memory structure**  Source: Kioxia, IEDM2024		**Alternative memory scheme**  Source: Kioxia, VLSI2023		
Stack image	CUA / CBA 		CBA 		CBA 		CBA 		CBA 	
WLC	VC 		VC		eWLC 		eWLC		eWLC	
CMOS	PolySi 		PolySi		HKMG (Gate Last) 		HKMG (Gate Last)		HKMG (Gate Last)	

Single-wafer cleaning for evolving DRAM and NAND processes

- Combining wafer cleaning and wet etching expertise, accommodating a range of device architecture, production, and processes, built over a half century.
- Accommodates wide-ranged evaluation during the development phase and smooth narrowing during the large-scale production phase.

Proven track records

- No.1 market share in single-wafer cleaning
- Supporting advanced Logic miniaturization
- Driving improvements in device yield

Features

- Multi-process chambers for loading several types of chemicals
- Acid, alkali, and organic chemicals can be loaded at the same time
- Allows to reclaim and reuse several types of chemicals
- Flexible chemical combinations possible with DDI*

*DDI: Dynamic Direct Injection

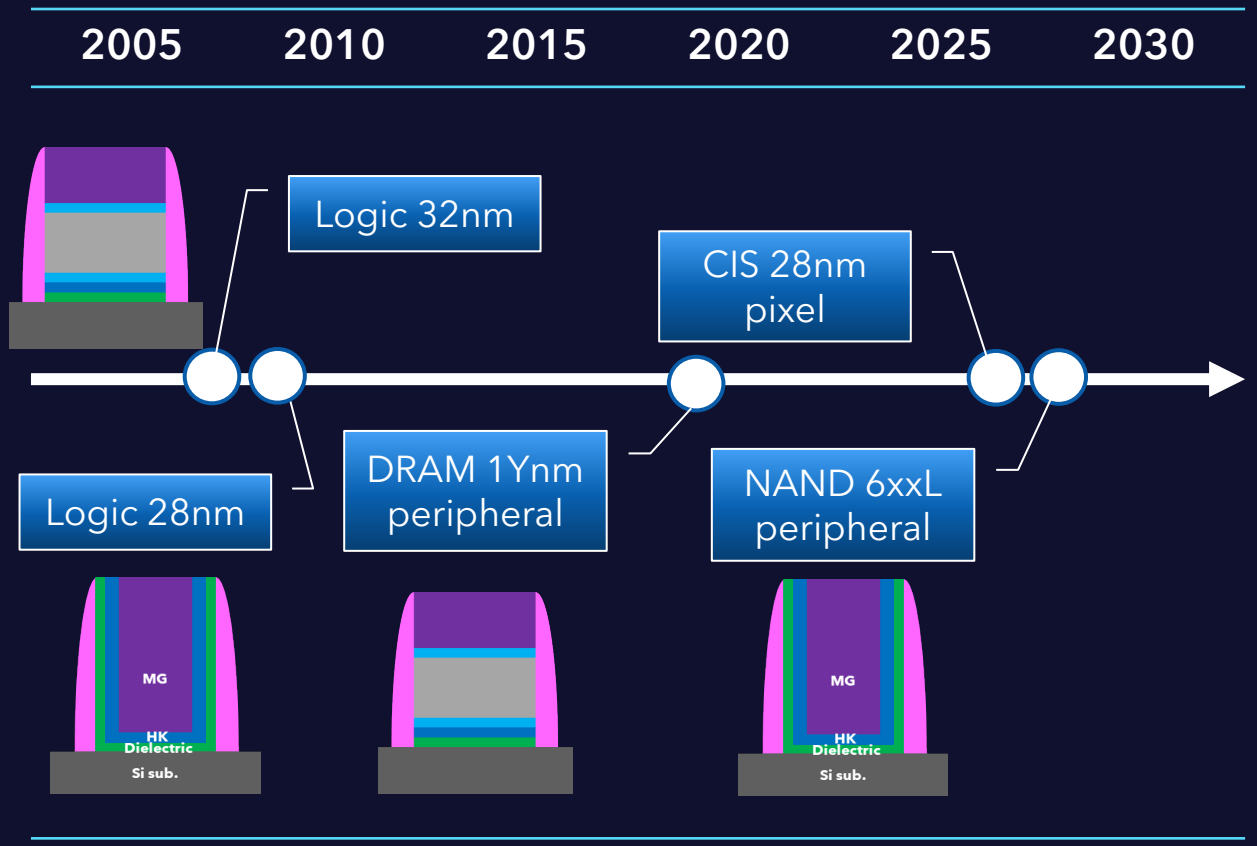
Process applications

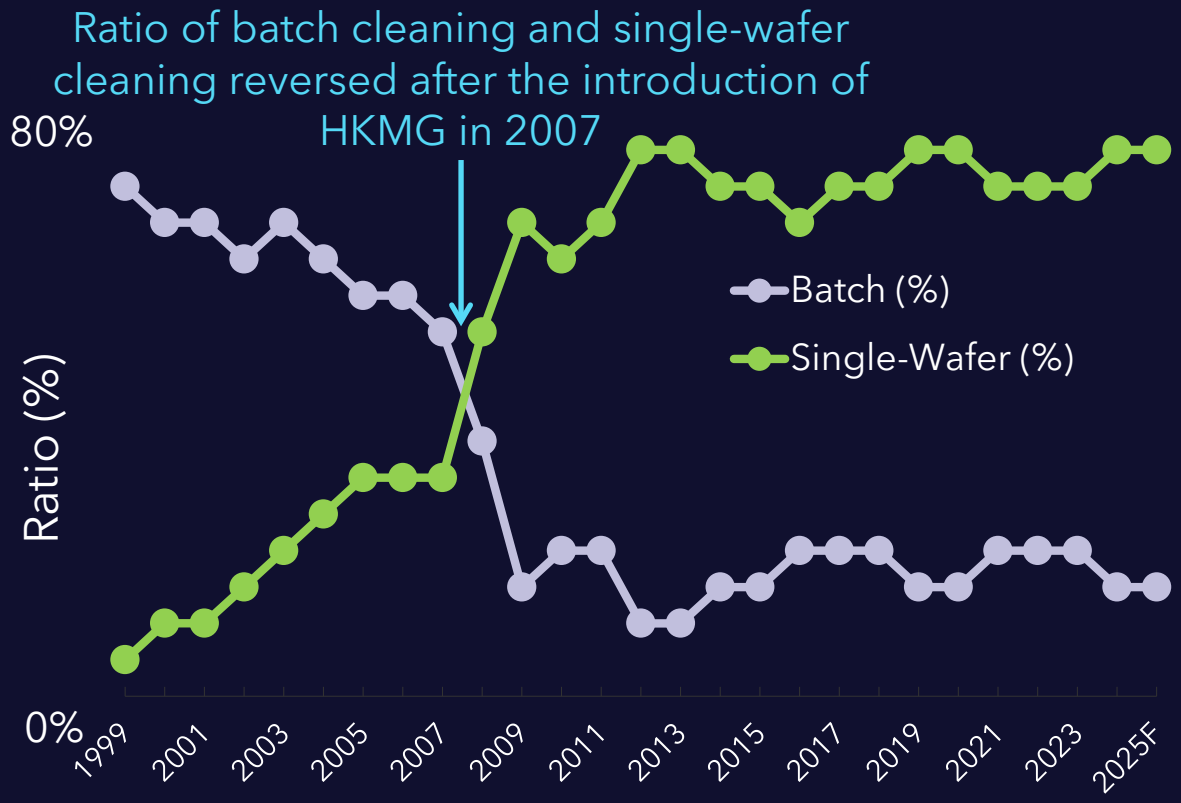
- HF, APM, HPM, etc. (mainly for particle removal)
  - ✓ Pre-deposition clean, post-deposition/dry clean
- SPM (mainly for resist, organic residue, and slurry removal)
  - ✓ Resist removal
  - ✓ Post-process clean (DRY, CMP)
- Wet etching (mainly for processing)
  - ✓ Metal etch
  - ✓ Oxide film etch
  - ✓ Si etch

HKMG: High-k Metal Gate

Single-wafer cleaning more in demand with HKMG integration

- HKMG-CMOS is increasingly adopted to accommodate the need for high-speed, energy-saving devices, in step with the AI revolution.
- Demand for single-wafer wet cleaning will increase further.



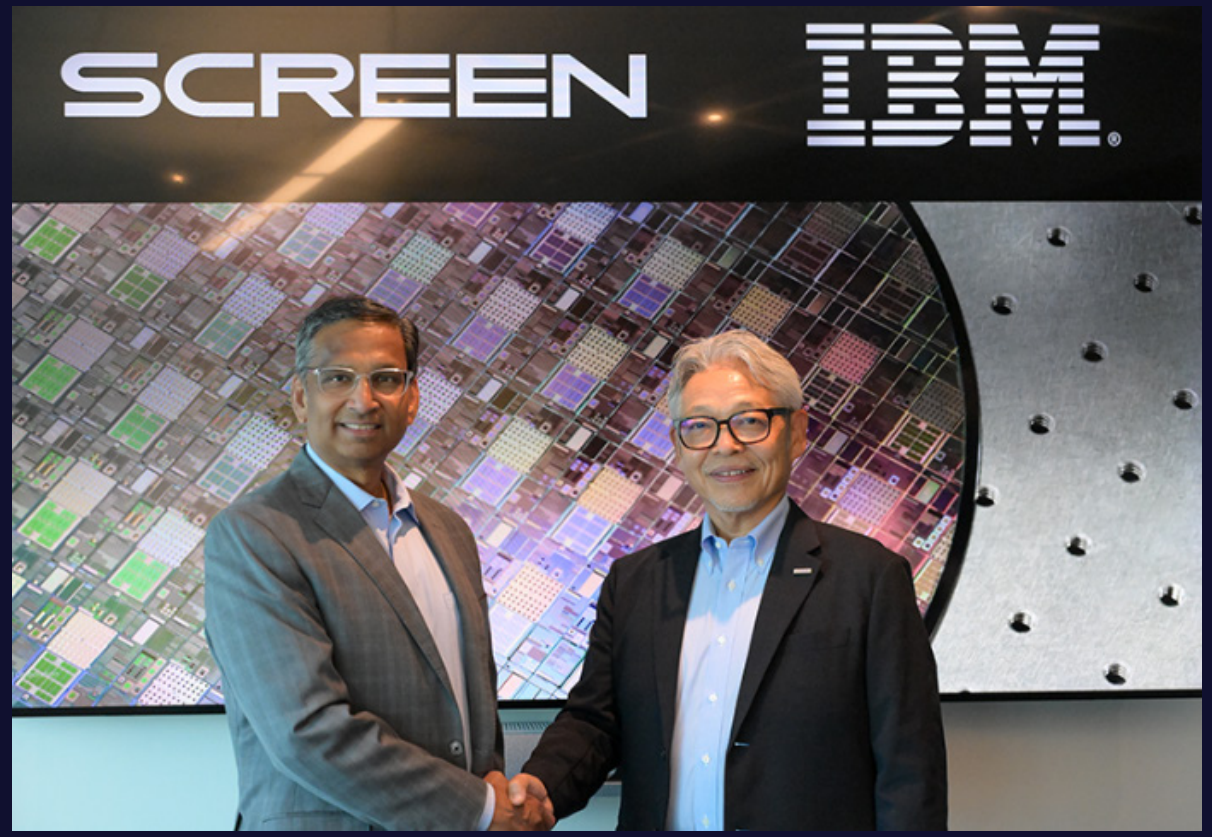


Source: Created based on Gartner data

Single-wafer wet cleaning are better suited to prevent cross contamination.

Joint R&D with IBM

Press release published September 24, 2025: *SCREEN and IBM Sign Agreement for Next-Generation EUV Lithography Cleaning Process Development - Agreement builds on more than a decade of collaboration between the two companies*



Left:
Dr. Mukesh Khare, GM of IBM Semiconductors and VP of Hybrid Cloud, IBM

Right:
Akihiko Okamoto, Representative Director and President of SCREEN Semiconductor Solutions

Off-shore R&D base, "ATCA," established in New York

Press release published December 16, 2025: *SCREEN to establish an R&D center in Albany, New York for semiconductor production processes*

ATCA will be located within Albany NanoTech Complex, the state-of-the-art semiconductor facility operated by NY Creates (NYCR).

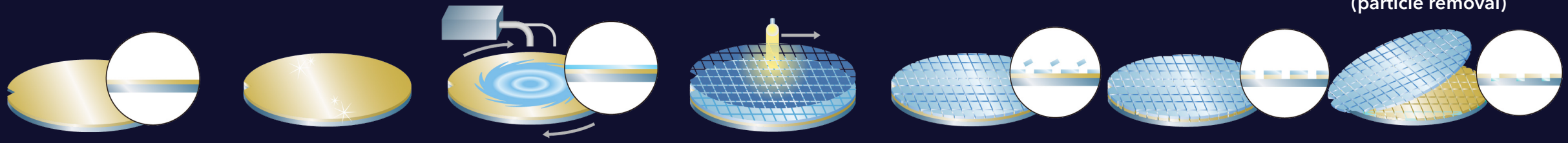
It will be using NYCR's clean room and other infrastructure to pursue solo research as well as joint research with global partners.

We will aim to increase our presence in wet cleans as well as thermal processing and advanced packaging.

Back-side and bevel cleaning: Growing importance in the EUV process flow

Back-side and bevel cleaning

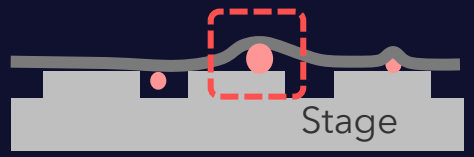
Film deposition | Pre-lithography clean | Resist coating | Lithography | Developer | Dry etch | Post-process clean (particle removal)



Particles

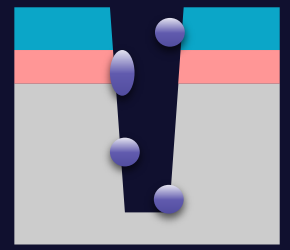
Scratch

Wafer



MOR

Metal contamination



Polymer residue

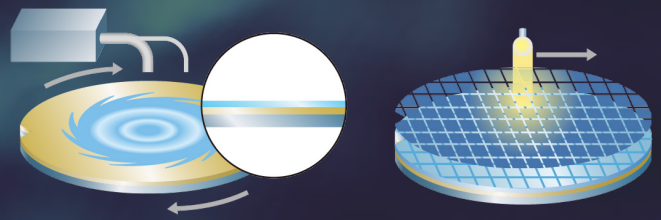
Back-side cleaning to maximize patterning performance

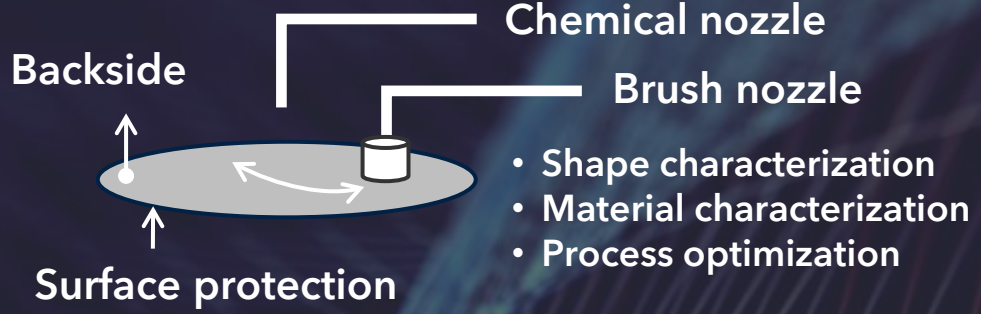
ATCA-related

Combining chemical and physical cleaning for optimal back-side processing

Back-side and bevel cleaning

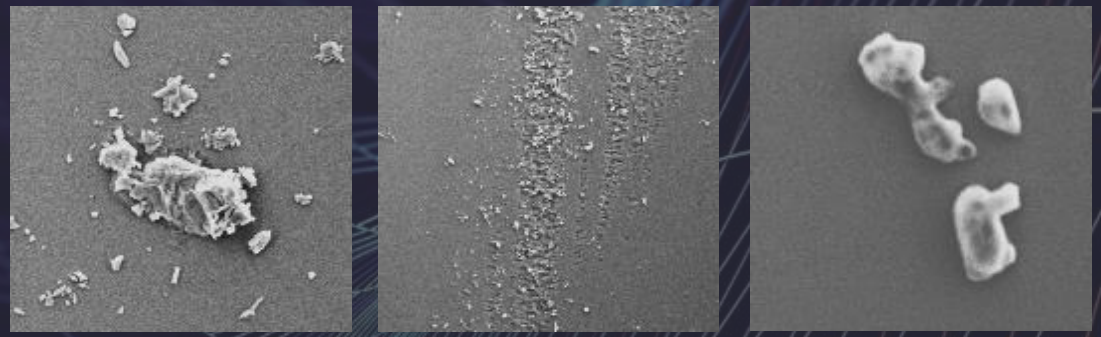
Resist coating → Lithography



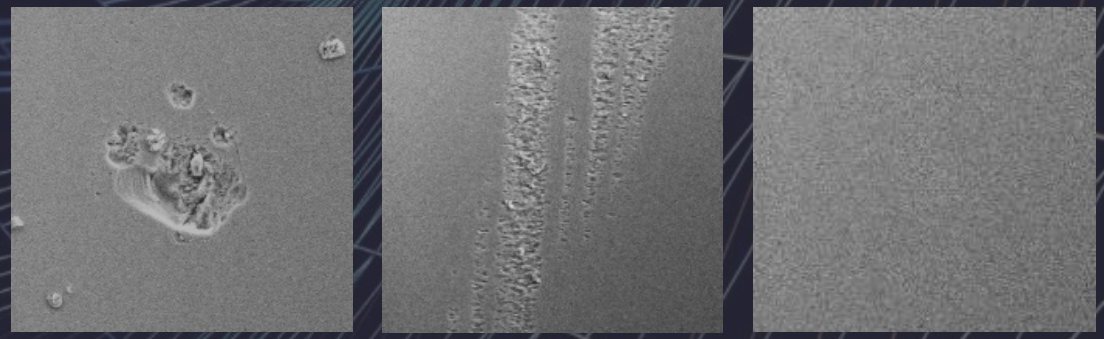


- Shape characterization
- Material characterization
- Process optimization

Before



After

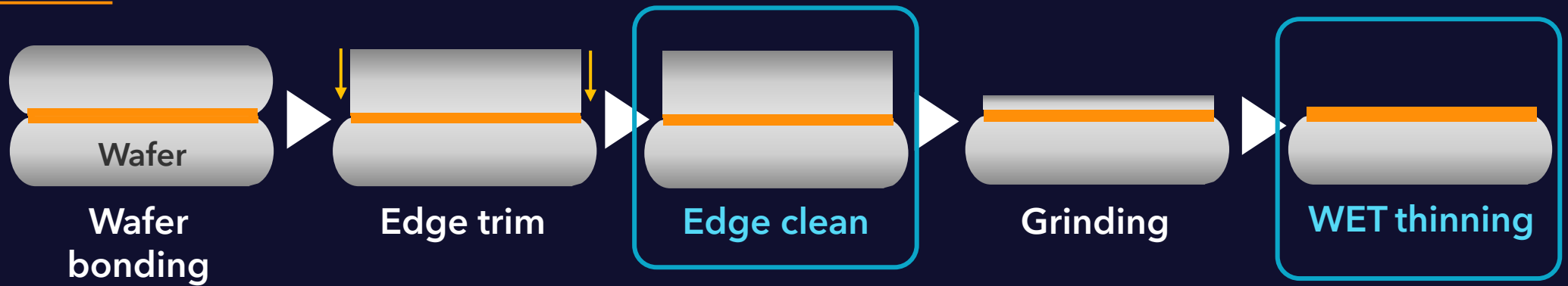


Source: SCREEN, SPCC2019

Wafer bonding process

Pre-bonding

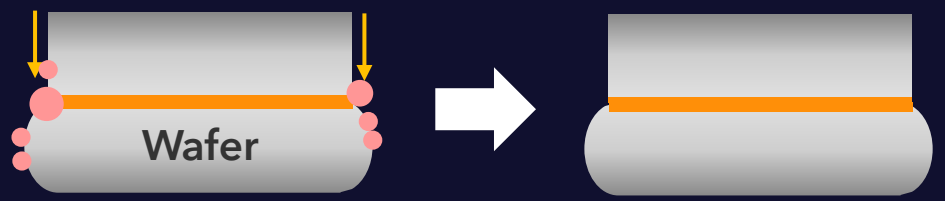
Post-bonding



Edge clean after wafer trimming

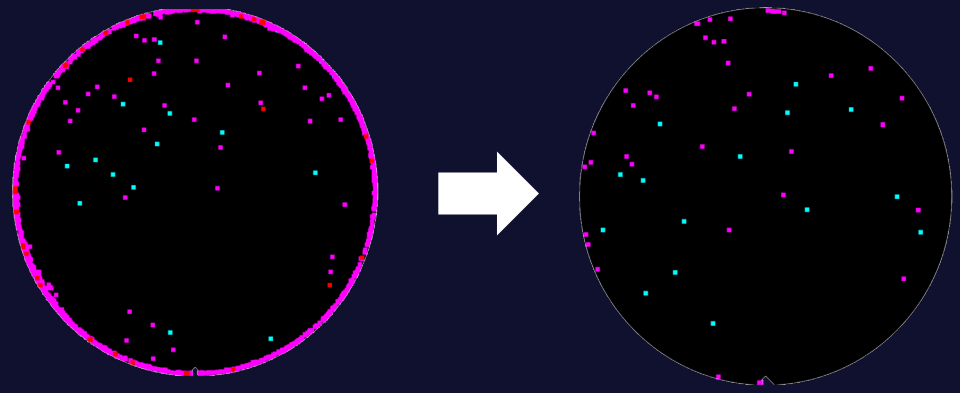
ATCA-related

Brush cleaning to remove particles on wafer edges



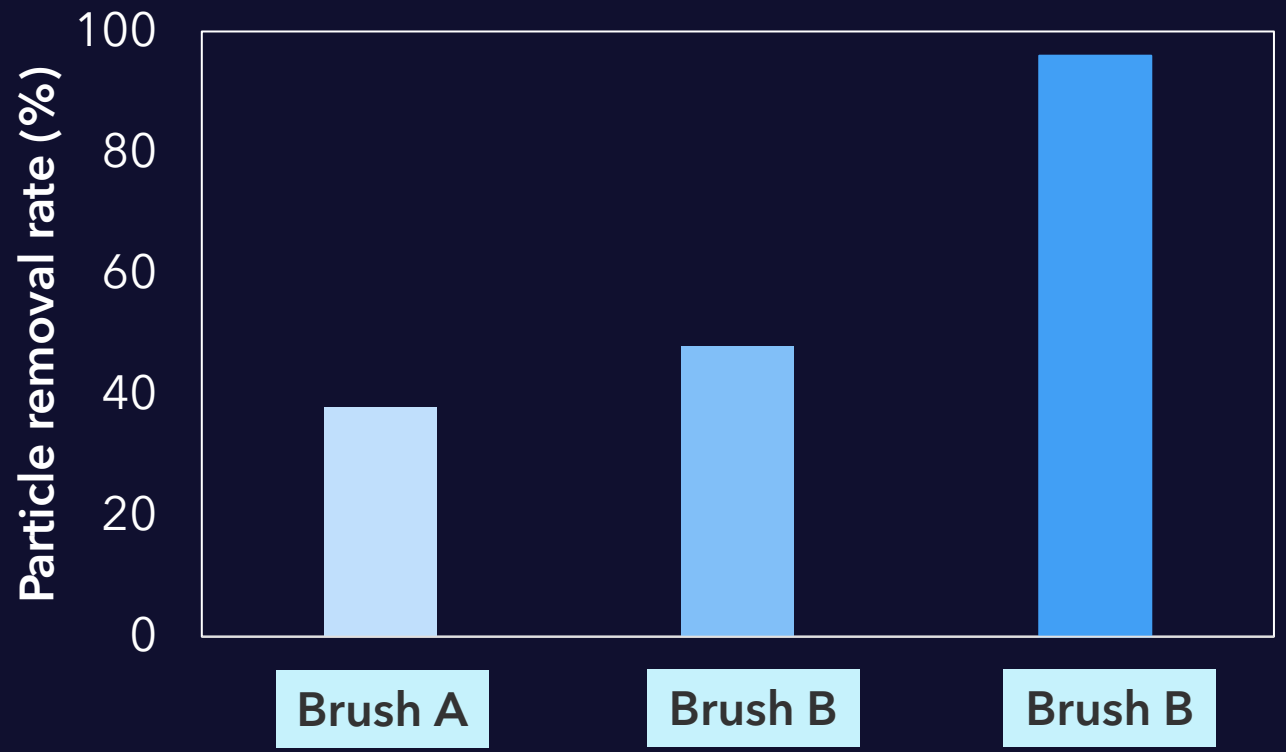
Edge trimming → Edge clean

Before → After



Brush nozzle

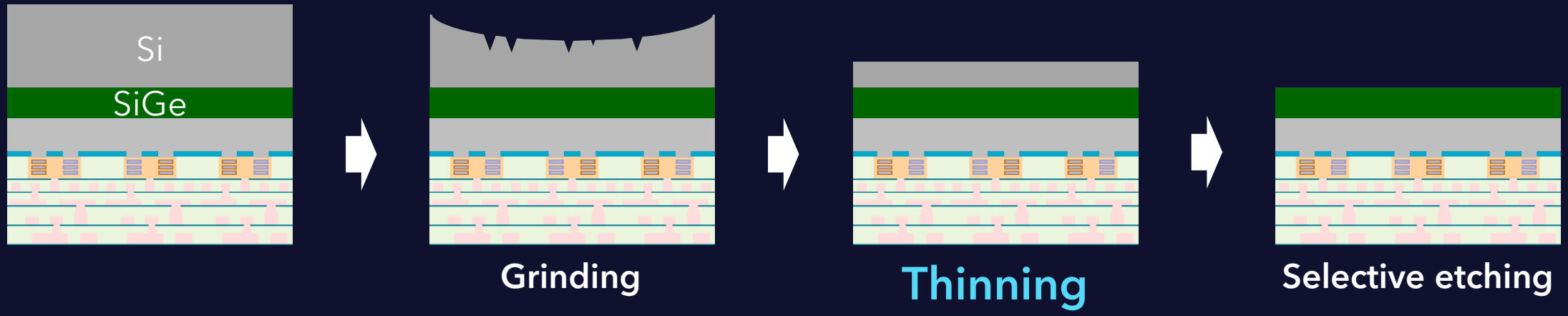
- Shape characterization
- Material characterization
- Process optimization

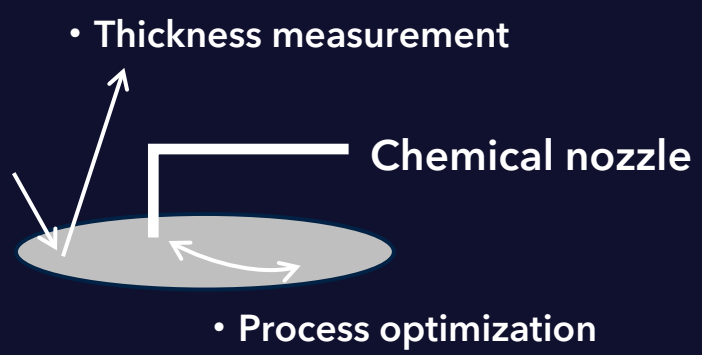


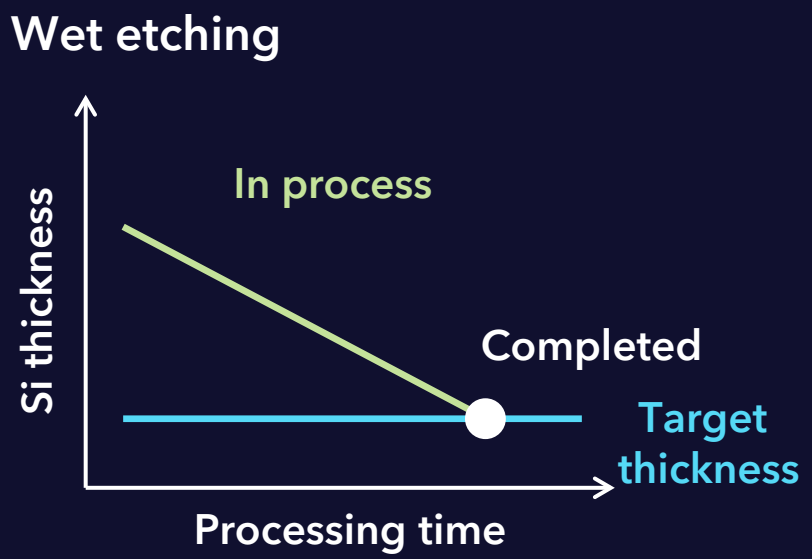
Wafer thinning after bonding

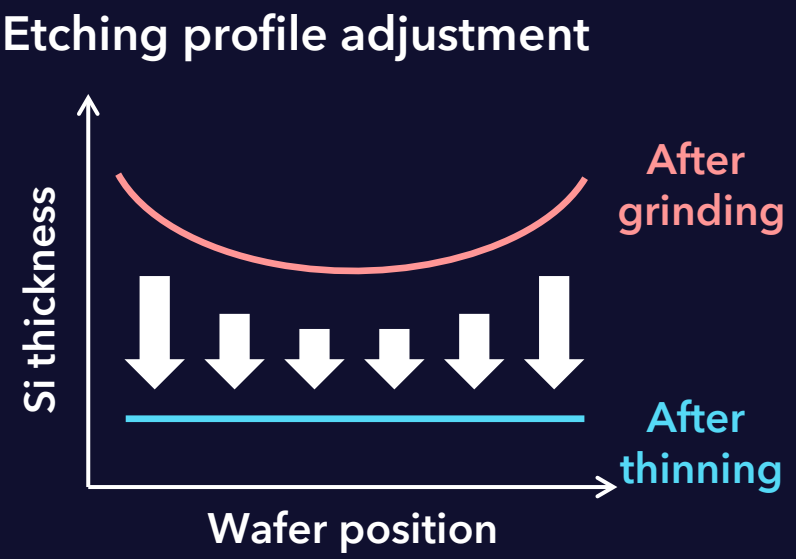
ATCA-related

Leveraging wet etching expertise and etching profile adjustment knowhow



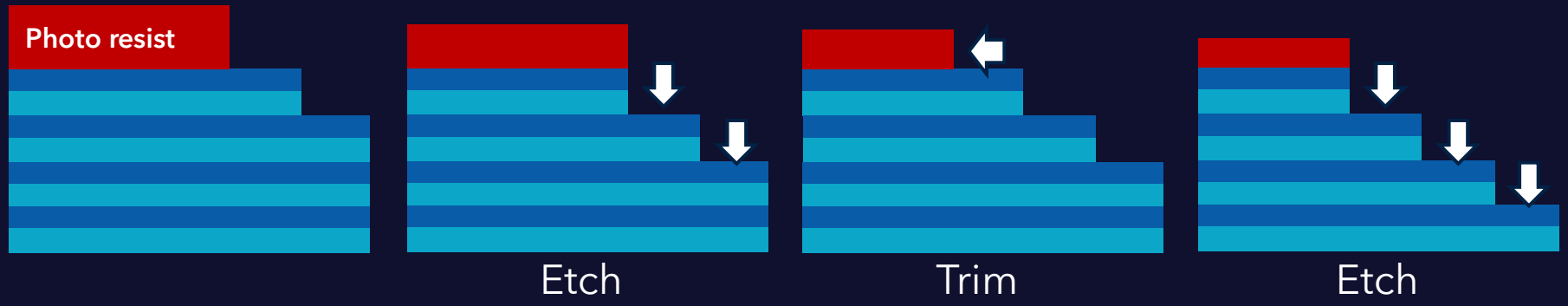




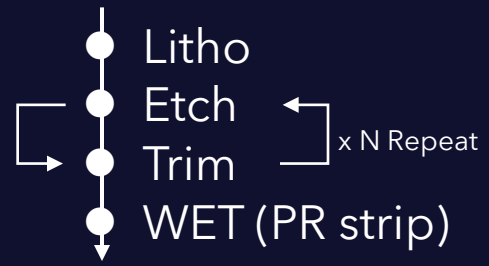


Single-wafer SPM more in demand with NAND eWLC process

- Conventional Process (w/ staircase)



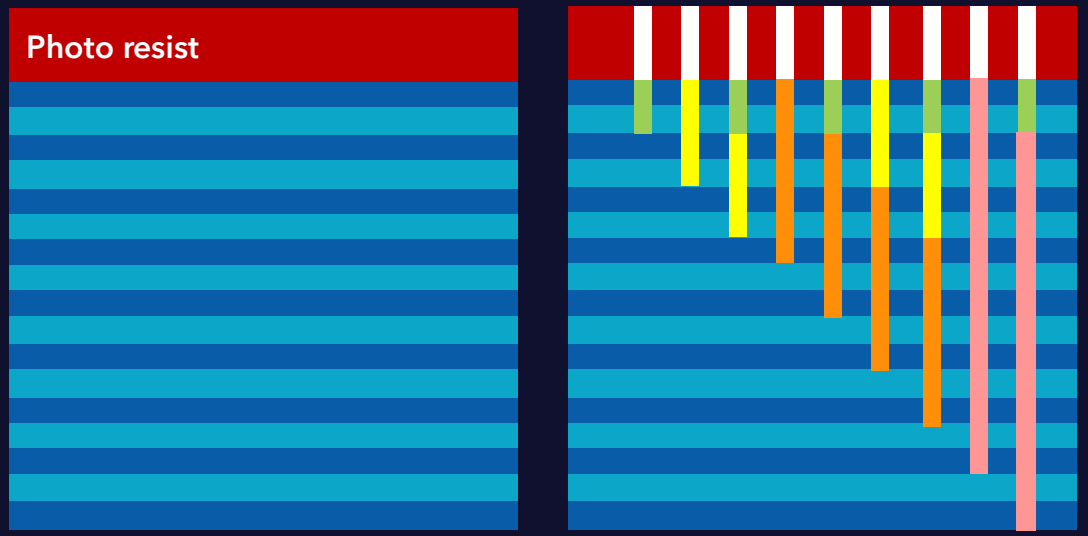
eWLC: exponential WL Contact



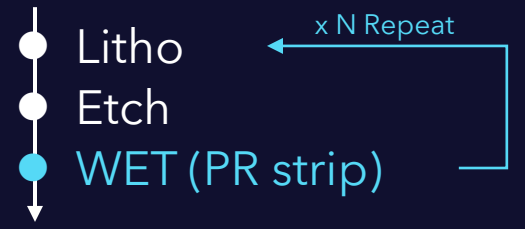
Batch WET

- eWLC process (w/o staircase)

* Estimated based on TechInsights data



# of etch	Etched layer
1	$2^0=1$
2	$2^1=2$
3	$2^2=4$
4	$2^3=8$



Single WET w/ reclaim SPM

Potential challenges

- Selectivity for stacking material
- PR removal
- **SPM chemical reduction**
- **SPM drain cost**

More opportunities to leverage our experience working with foundries

Summary

Aiming for further growth in wet cleaning leveraging our technological excellence

HKMG

High-NA EUV

Wafer Bonding

Novel Structure

New material

New architecture

A Better Tomorrow
With Our Partners

Advanced packaging trends and outlook

SCREEN Semiconductor Solutions Co., Ltd.

Joichi Nishimura
General Manager, Engineering and Marketing
Advanced Package Department (ADPKG)

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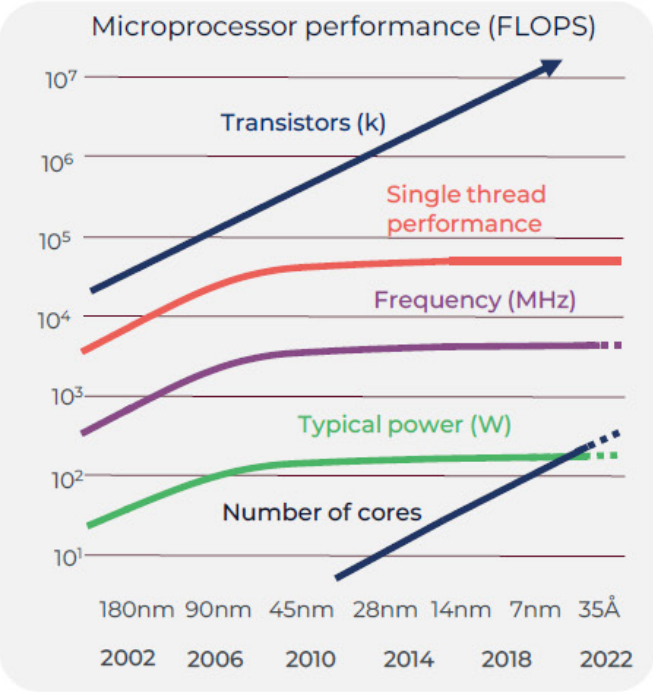
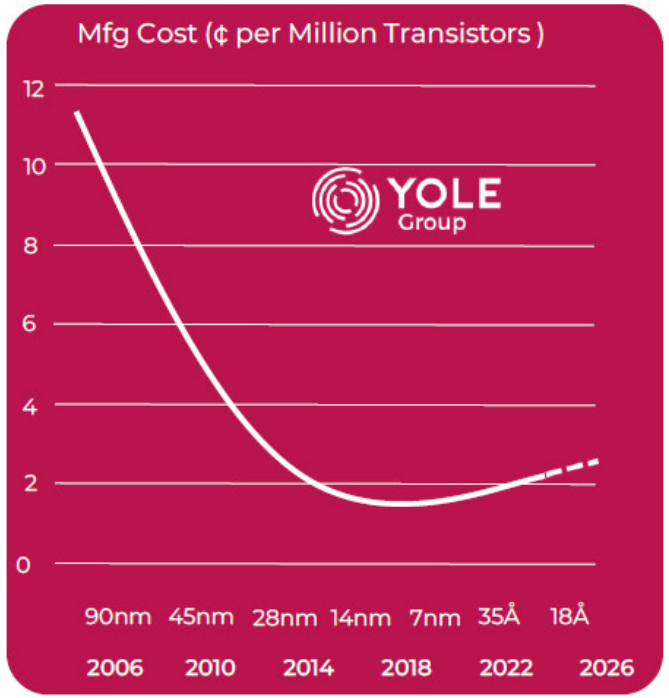
Why is advanced packaging important?

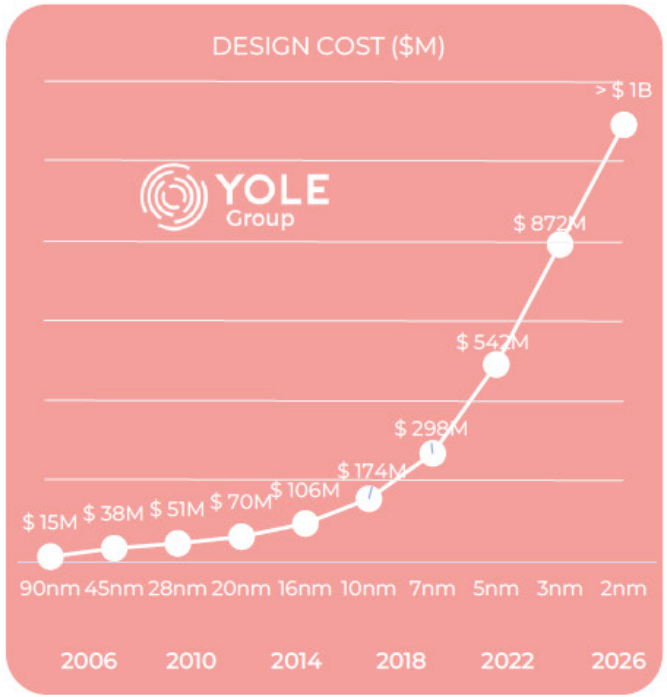
Challenges:

- The slowdown of Moore's Law
- While miniaturization has increased transistor density, performance gains have plateaued, and power consumption continues to rise.
- The reduction in manufacturing costs has already reached its limit, while design costs continue to rise.

To overcome these challenges, leveraging advanced packaging technologies has become essential.

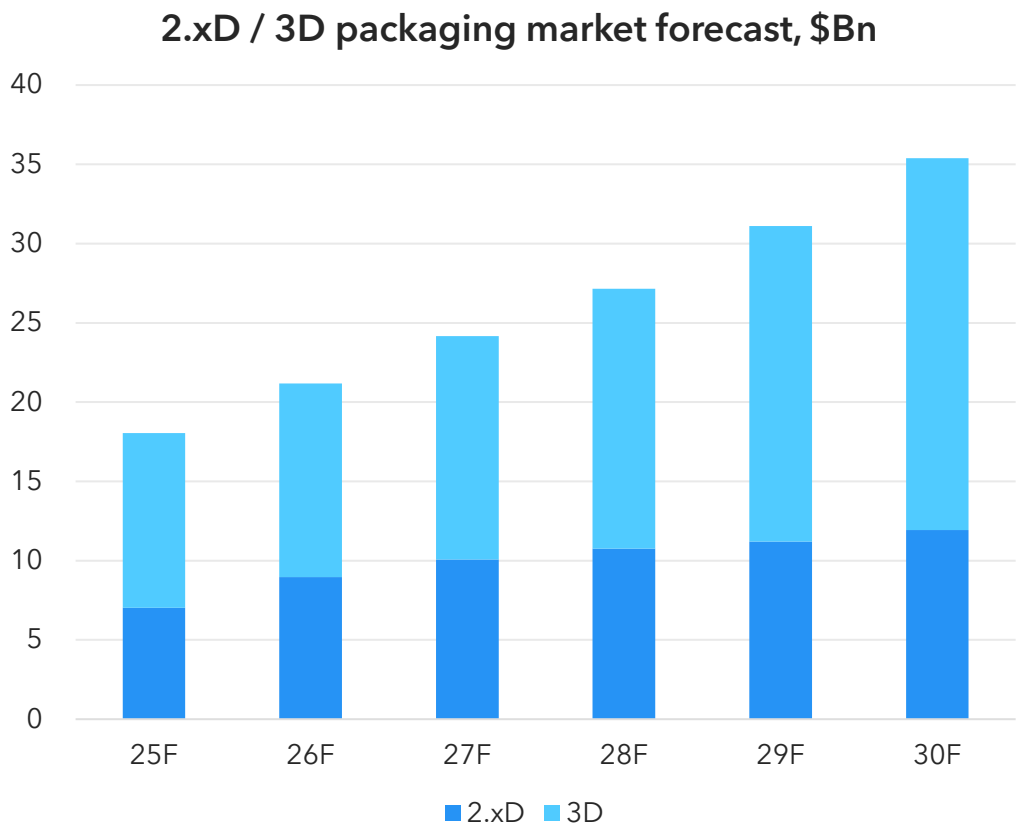






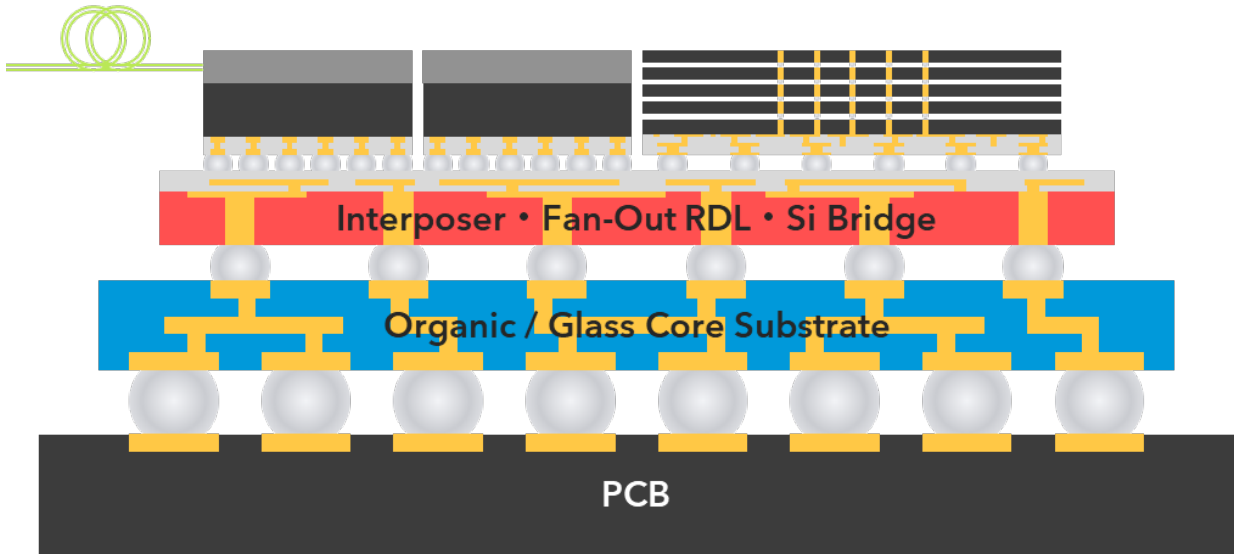
Data from High-End Performance Packaging 2025 – Yole Group

2.xD and 3D packaging: market trends and key focus areas



Data from Advanced Packaging Market Monitor, Q2 2025 – Yole Group

The 2.xD and 3D packaging markets are expected to maintain strong growth momentum.



Key focus areas:

- 3D packaging solutions: development (WoW bonding system, etc.)
- 2.xD packaging solutions: development and marketing

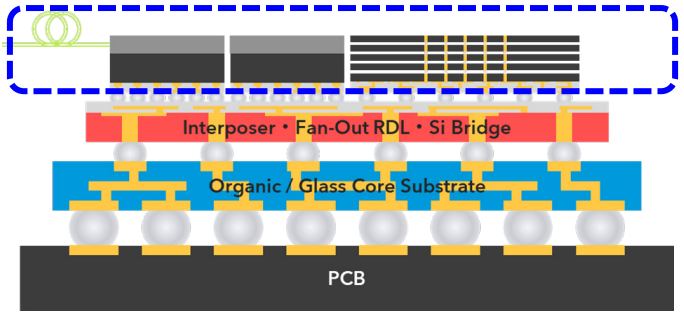
Initiatives in 3D packaging

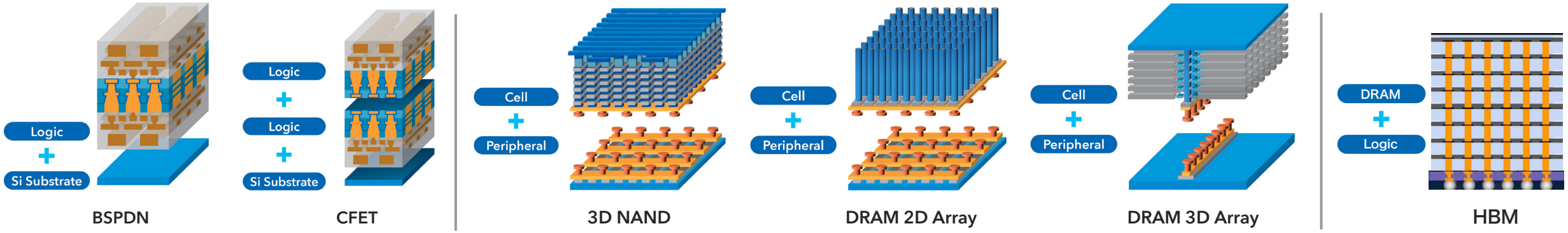
Accelerating development of 3D packaging solutions

WoW bonding systems

Development started in FY2021 as part of the NEDO project

- Proprietary plasma (LIA) technology enabling low-temperature Cu-Cu bonding
- Integrated in-house cleaning unit (spin scrubber)
- Advanced wafer transfer control technology





Peripheral process equipment

Ongoing development of systems for processes and inspections related to WoW and CoW bonding

As WoW bonding is adopted in logic and memory devices, its applications are expected to grow significantly, driving greater demand for associated process and inspection solutions.

Acquisition of an R&D business in wafer bonding from Nikon

(effective on September 30, announced October 31, 2025)

SCREEN

SCREEN Holdings

News Release

October 31, 2025

Acquisition of an R&D business in wafer bonding from Nikon

SCREEN Holdings Co., Ltd. (SCREEN HD, President & CEO: Masato Goto) hereby announces the acquisition of an R&D business in wafer bonding from Nikon Corporation (Nikon; headquarters: Tokyo; Representative Director and Chairman: Toshikazu Umatate), effective on September 30.

In the semiconductor advanced packaging field, expectations are rising for more high-precision wafer bonding to support the increasing demand for footprint- and energy-saving devices. Positioning advanced packaging as a focus field, in addition to the sales of direct imaging systems and coater/dryer systems, we are working on the development and roll-out of low-temperature wafer bonding. The latest acquisition will allow us to combine Nikon's ultra-high-precision bonding technology with our proprietary technology as we seek to lead the world in bonding technology and establish a presence in this field.

Under the current medium-term management plan, Value Up Further 2026, covering the three fiscal years ending March 2027, SCREEN has been investing intensively for growth. In particular, we focus on advanced packaging as a new business field with a high growth potential, leading to the latest acquisition. The acquisition has already been reflected in the business plan for this fiscal year and therefore will not impart our earnings forecasts.

SCREEN will continue serving diverse client needs in the semiconductor packaging industry and contribute to its further development.

Overview of the acquisition

1. Acquired business	Nikon's R&D business in wafer bonding
2. Acquired from	NIKON CORPORATION Headquarters: 1-5-20 Nishioi, Shinagawa-ku, Tokyo, Japan Representative Director and Chairman: Toshikazu Umatate Capitalization: JPY 65,476 million (as of March 31, 2025) Established: July 25, 1917
3. Date of agreement	August 14, 2025
4. Date of acquisition	September 30, 2025

Nikon

NIKON CORPORATION

Information

Transfer of research and development business for semiconductor wafer bonding technology

October 31, 2025

TOKYO - Nikon Corporation (Nikon) announced that it has entered into a transfer agreement with SCREEN Holdings Co., Ltd. (SCREEN) regarding Nikon's research and development business for semiconductor wafer bonding technology as follows.

Background of the transfer

Wafer bonding is a technology that is attracting attention as a way to improve semiconductor performance. SCREEN and Nikon have been discussing future collaborations regarding this technology. As a result, Nikon has concluded that transferring the technology to SCREEN is the best option, leading to the signing of this agreement. Nikon and SCREEN will continue to strengthen our collaboration, aiming to further refine the technology and quickly implement it in actual semiconductor manufacturing.

Transfer details

Nikon's semiconductor wafer bonding technology, know-how, intellectual property, etc.

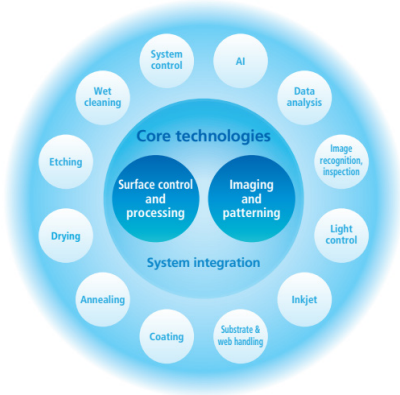
Overview of the transferee

Company name	SCREEN Holdings Co., Ltd.
Head office location	Tenjinkita-machi 1-1, Teranouchi-agaru 4-chome, Horikawa-dori, Kamigyo-ku, Kyoto, Japan
Representative	Masato Goto, President and Chief Executive Officer (CEO)
Capitalization	54.0 billion yen (As of March 31, 2025)
Date of establishment	October 11, 1943

Source: News releases of the respective companies.

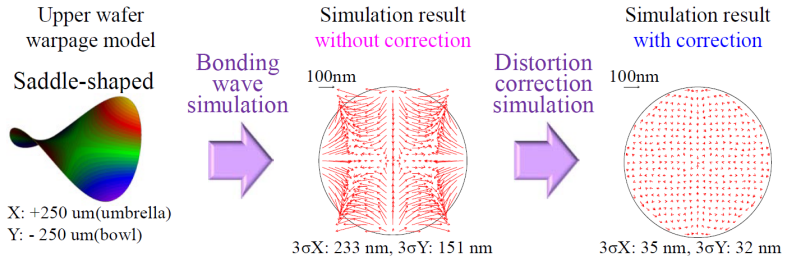
Advantages of our wafer-on-wafer (WoW) bonding system

Nikon × SCREEN



Nikon's ultra-high precision alignment units leveraging the FEOL exposure technology

Distortion removal mechanism



Source: H. Mitsuishi et al., "50 nm Overlay Accuracy for Wafer-to-wafer Bonding by High precision Alignment Technologies," 2023 IEEE 73rd Electronic Components and Technology Conference

SCREEN's wet clean units (spin scrubbers)

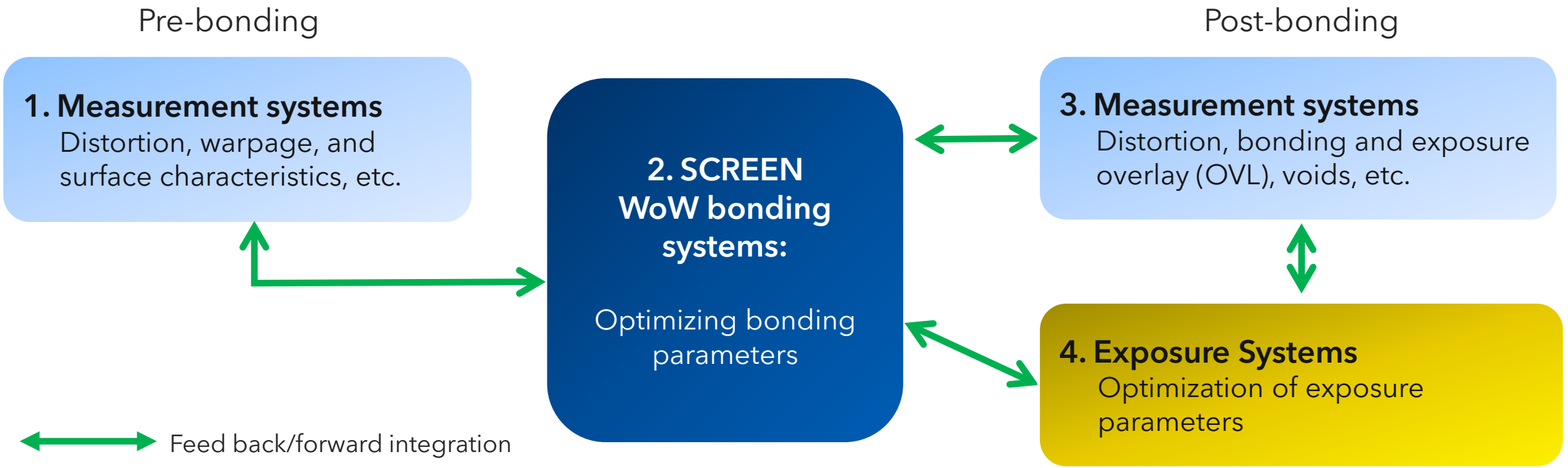
Plasma technology (LIA) enabling
low-temperature Cu-Cu bonding

* Enable the formation of an oxide-free, active Cu bonding surface with minimal damage

Wafer transport system

By combining both technologies, we are positioned to address the evolving market demands for WoW bonding systems, which are expected to become increasingly advanced and complex.

Feed back/forward integration across process steps

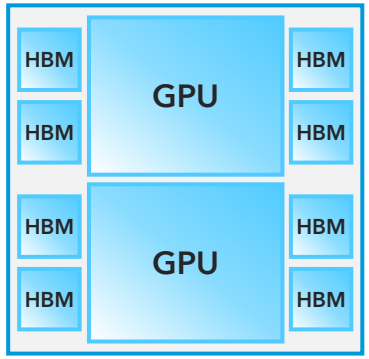


With increasingly stringent bonding accuracy requirements, demand for single-wafer optimization is rising. Driving innovation with a focus on integration with peripheral processes and metrology systems.

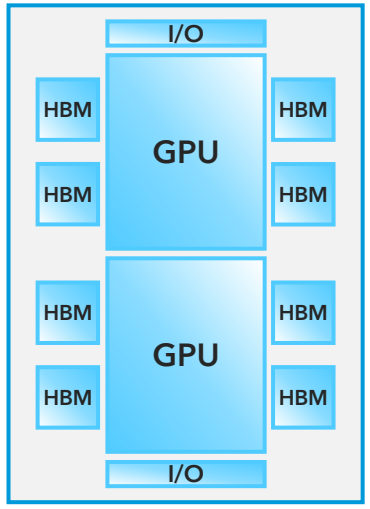
Initiatives in 2.xD packaging

Ongoing shift toward larger chip sizes

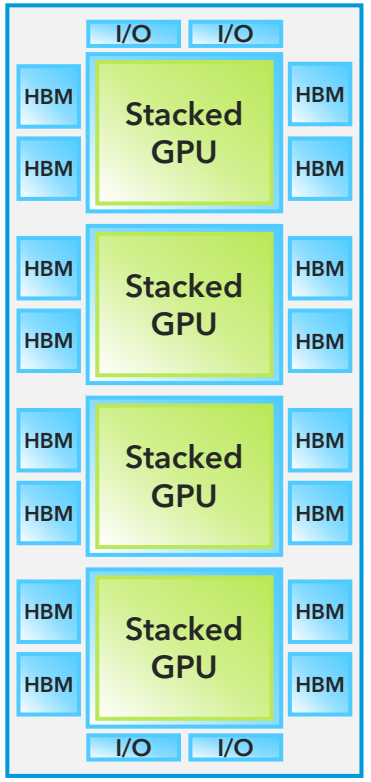
CY25 → CY26 → CY27 → CY28



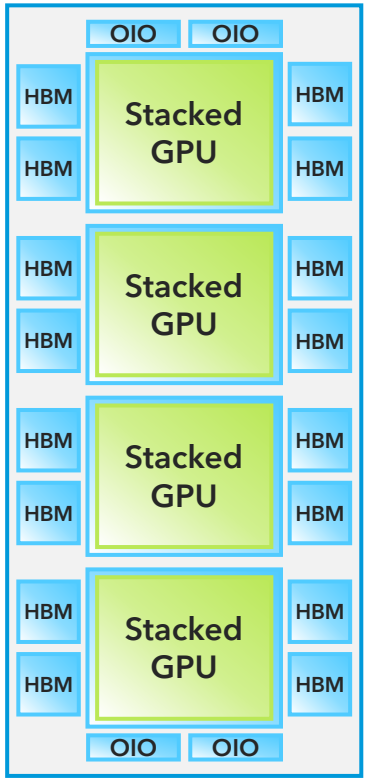
2 GPU, 8 HBM
3.3x Interposer
80x80mm Substrate



2 GPU, 8 HBM, 2 I/O
5.5x Interposer
100x100mm Substrate



4 GPU w/ 3D SRAM, 16 HBM, 4 I/O
9.5x Panel Interposer
120x150mm Substrate



4 GPU w/ 3D SRAM,16 HBM, 4 Optical I/O?
9.5x Panel Interposer
120x150mm Substrate

The ongoing increase in chip size will further elevate the importance of PLP.

2.xD solutions

LeVina

LeVina: Direct imaging system for next-generation patterning

Exposure area

LeVina-h	≦ 620 x 650mm
LeVina-i	≦ 620 x 650mm

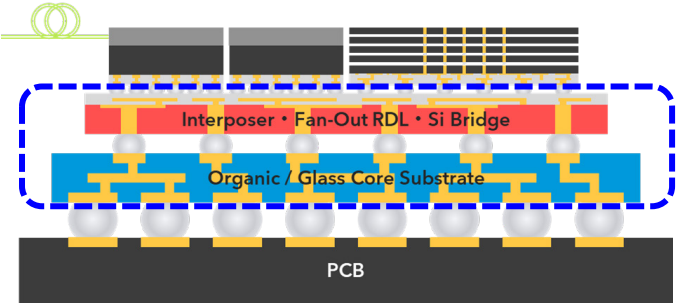
LEMOTIA

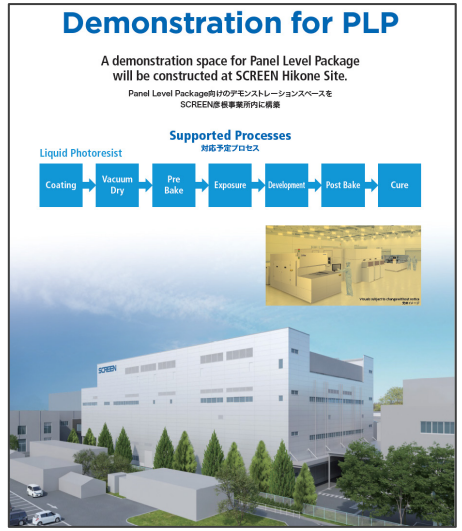
Lemotia: Slit coater system for panel-level packaging (PLP)

New

Panel size

LM-6000	600 x 600mm or 510 x 515mm
LM-3000	310 x 310mm or 300 x 300mm





A demonstration space currently under construction in the Hikone Site—providing seamless solutions for the PLP processes

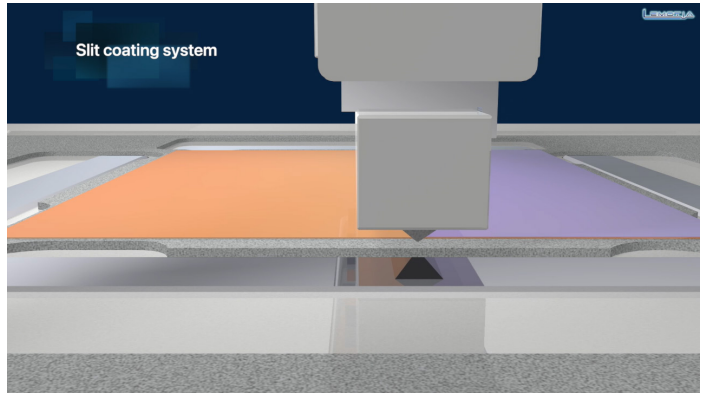
Strengthening efforts in 2.xD solution development and marketing; Lemotia has launched new offerings for 300 mm and 310 mm panels.

Spin coater vs slit coater: Comparison

	Spin Coating	Slit Coating
Consistency	Difficult to coat corner edge	Compliant with the PLP standard ✓
Thick film coating	Difficult	Possible ✓
EBR	Required & difficult (Due to warpage)	Not required ✓
Low-pressure drying	Not required ✓	Required
Chemical usage	Large amount	Small amount ✓
Distortion adjustment	Required to develop	Already available ✓
Panel size expandability	Required to develop	Proven in the FPD market ✓

Note: Comparison based on SCREEN's in-house experiment.

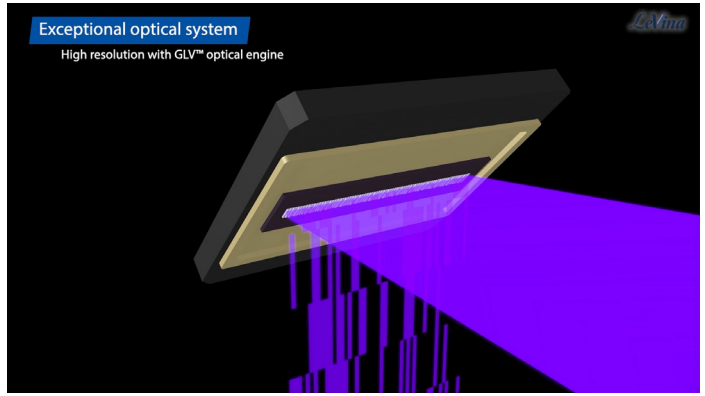
LEMOTIA



Slit coater is better suited for panel coating due to consistency, less chemical use, and capability to adjusts panel distortion, accommodating the future expansion of panel size.

Our exposure systems

Application	PLP/WLP	PLP	PLP	FCBGA/FCCSP/ MCM	FCBGA/MCP	FCCSP/MCM
Wavelength	375nmLD	375nmLD	405nmLD	405nmLD	Broad	Broad
Model	DW-3100 	LeVina-i 	LeVina-h 	LUPIOS 	Ledia Qs 	Ledia 8F 
Productivity						
Resolution (L/S)	 ≦ 1/1µm	 2/2µm	 5/5µm	 8/8µm	 10/10µm	 12/12µm
Maximum Exposure Area	310 × 310 mm	620 × 650 mm	620 × 650 mm	546 × 635 mm	587 × 661 mm	610 × 661 mm
Overlay (Ave + 3α)	 0.5µm	 2.0µm	 3.5µm	 3.5µm	 5µm	 5µm



LeVina and the DW series feature SCREEN's GLV™ optical engine

Expanding our product lineup further to address diversified exposure needs in advanced packaging.

Summary

Increasing SCREEN's presence and business scale in advanced packaging

2.xD	Focusing on expanding the product lineup of exposure and coater/dryer systems and their marketing
3D	Accelerating the development of WoW bonding systems as well as peripheral systems

Innovation for a Sustainable World