SCREEN Holdings Co., Ltd.

IR Day of the fiscal year ending March 31, 2026

Part 2

Event Summary

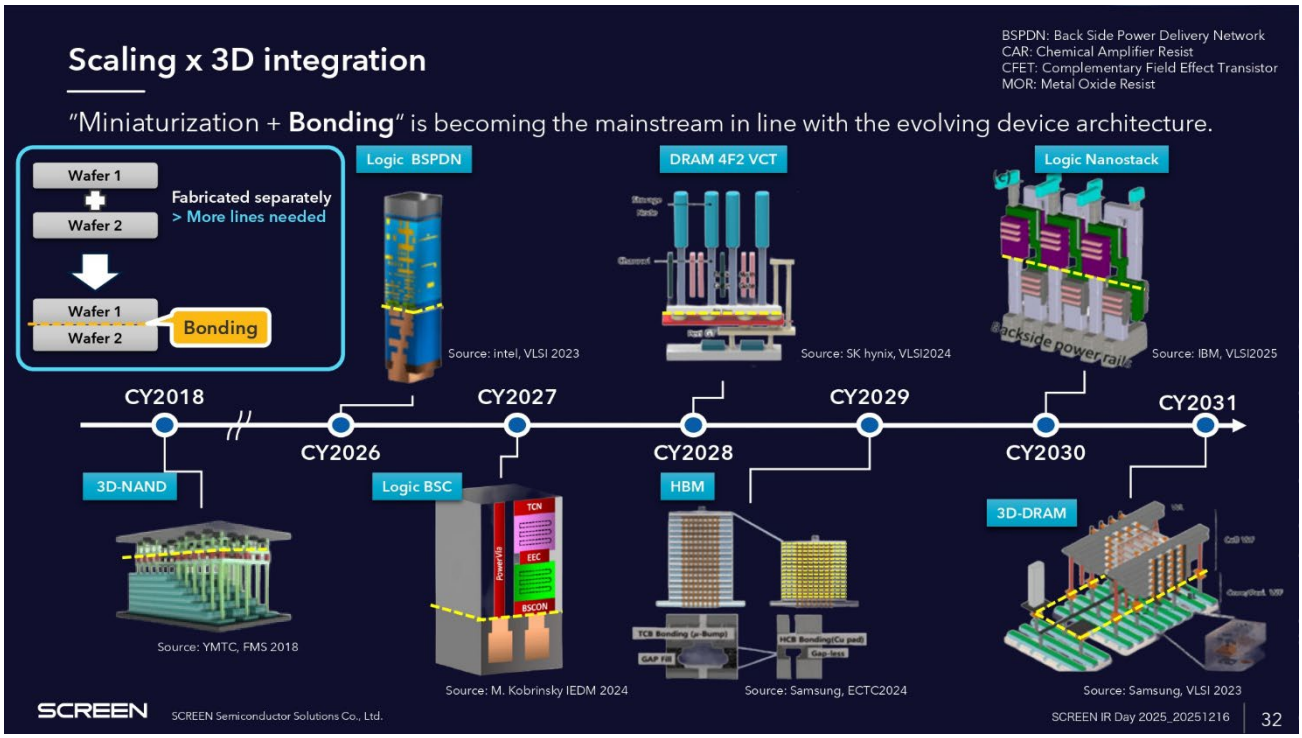
[Company Name]	SCREEN Holdings Co., Ltd.	
[Company ID]	7735-QCODE	
[Event Language]	JPN	
[Event Type]	Investor Conference	
[Event Name]	IR Day of the fiscal year ending March 31, 2026 (second half)	
[Fiscal Period]		
[Date]	December 16, 2025	
[Number of Pages]	34	
[Time]	16:30 – 17:36 (Total: 66 minutes, Presentation: 41 minutes, Q&A: 25 minutes)	
[Venue]	Webcast	
[Venue Size]		
[Participants]		
[Number of Speakers]	5	
	Akihiko Okamoto	Representative Director President, SCREEN Semiconductor Solutions Co., Ltd.
	Mikawa Takumi	Executive Officer, Intellectual Property Strategy Relations, Technology Strategy Relations, SCREEN Semiconductor Solutions Co., Ltd.
	Hiroaki Takahashi	Managing Director, R&D Strategy, SCREEN Semiconductor Solutions Co., Ltd.
	Joichi Nishimura	General Manager, Engineering and Marketing Advanced Package Department
	Yuichi Miura	General Manager, Investor Relations, Corporate Communications Department, Corporate Strategy Division
[Analyst Names]*	Atsushi Yoshioka	Nomura Securities

Shuhei Nakamura	Goldman Sachs
Masahiro Nakanomyo	Jefferies
Tetsuya Wadaki	Morgan Stanley MUFG Securities
Yu Yoshida	CLSA Securities

*Analysts that SCRIPTS Asia was able to identify from the audio who spoke during Q&A or whose questions were read by moderator/company representatives.

Presentation

Miura: Next, Mr. Takahashi, Managing Director, R&D Strategy, SPE, will explain SPE cleaning technology trends. Managing Director Takahashi, if you would, please.



Takahashi: Hello, everyone. I would like to briefly talk about SPE cleaning technology trends.

First, regarding the overall picture, this is a lineup of figures showing the transitions, or roadmaps, of various devices toward 2031, as presented by various companies in discussion papers.

I have placed 3D-NAND on the left, which began in 2018, and what these figures shown here have in common as shared characteristics are scaling and bonding.

It is a bit hard to see, but the surfaces where bonding is actually performed in each figure are indicated by these yellow dashed lines, and bonding has progressed significantly in all devices.

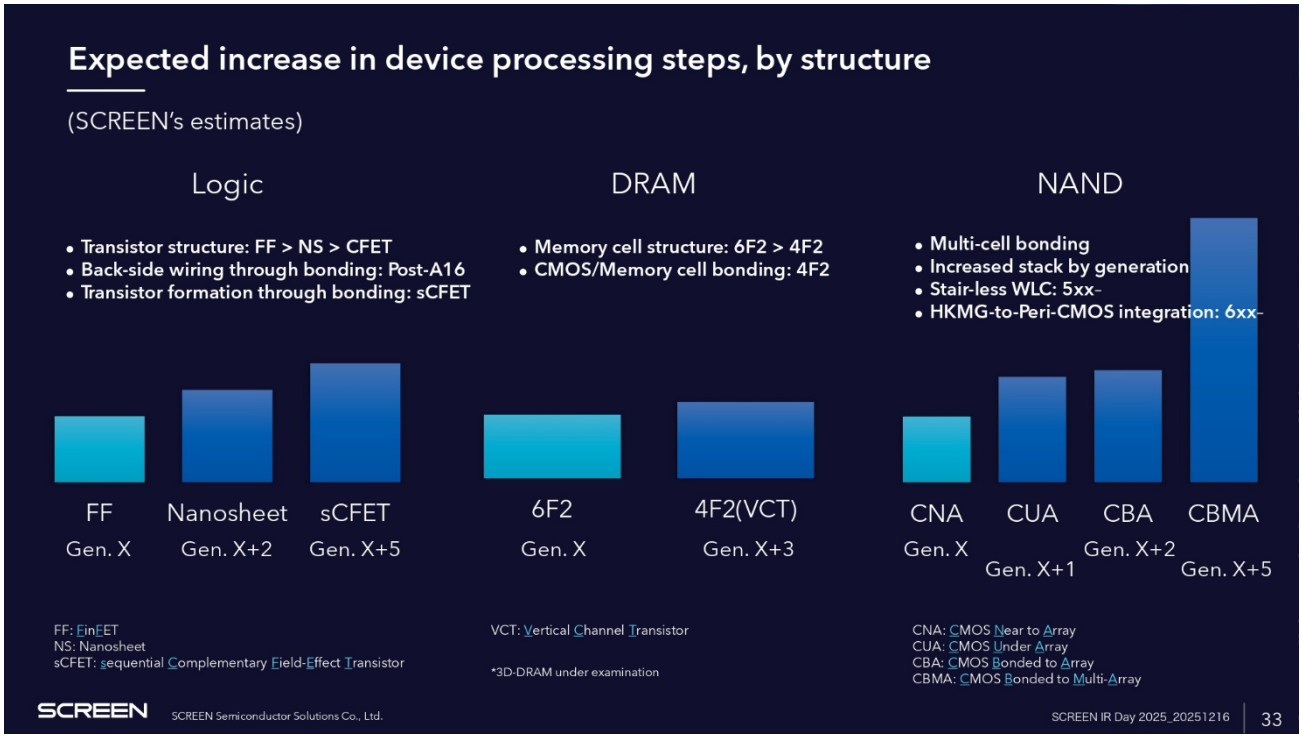
Along with that, as written on the left, wafers are produced on separate lines and then bonded together, and since they are naturally produced separately, an increase in the number of lines could also become a tailwind for us as a manufacturing equipment manufacturer.

Another point, looking back by device, it started with NAND, but in all devices, for example, in Logic, there is backside BSPDN and backside contact, and in DRAM, there is the transition from 6F2 to 4F2, and HBM for AI is also ramping up significantly.

In addition, what comes next for Logic? There is the question of how prototyping will proceed when it comes to CFET, but what IBM is saying here is that, under the name Nanostack, Logic will be stacked vertically.

At the bottom right, it says DRAM at the top, and this is also DRAM that lies beyond 4F2.

In response to the evolution of these devices, we are analyzing what challenges and what opportunities there are from a wet clean perspective.

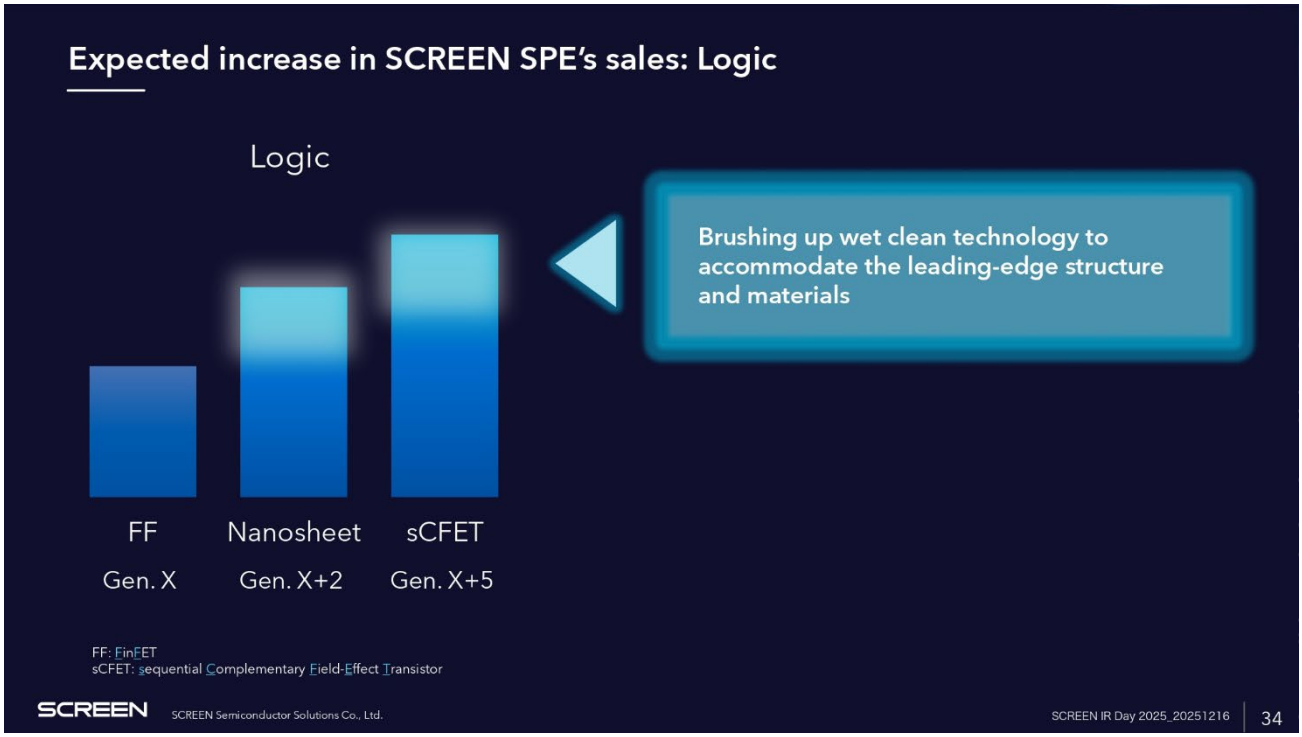


This single slide provides a concise summary, and it is an image of how we expect the number of cleaning process steps to change by device structure. From left to right, we have Logic, DRAM, and NAND, and the light blue area on the far left should be regarded as the initial generation. Then, as devices evolve, the number of cleaning process steps increases, which is what we are explaining.

Specifically for Logic, the number of cleaning process steps increases due to changes in structure, an increase in double-sided formation processes, and, as indicated by sequential and CFET, manufacturing devices by bonding wafers together.

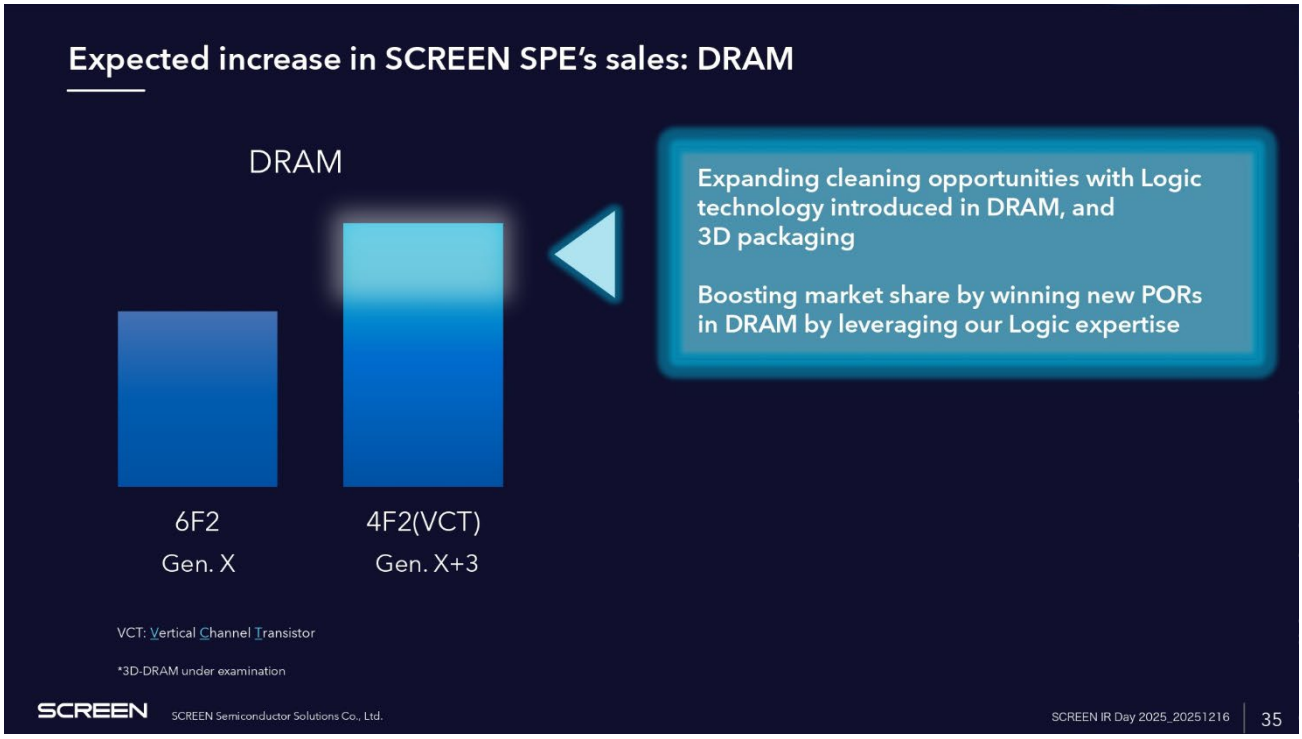
Turning to DRAM, the memory cell structure changes from 6F2 to 4F2, and as a result, the number of process steps increases due to bonding between CMOS and memory cells.

The same can be said for NAND. Bonding of multiple memory cell layers will progress, and the number of stacked layers itself will also increase. In addition, as is a characteristic of NAND today, the transition in how word line contacts are formed will likely have a major impact. Integration is also being considered for peripheral circuits, such as the introduction of High-k Metal Gate, so we assume that cleaning opportunities will expand significantly in these areas.



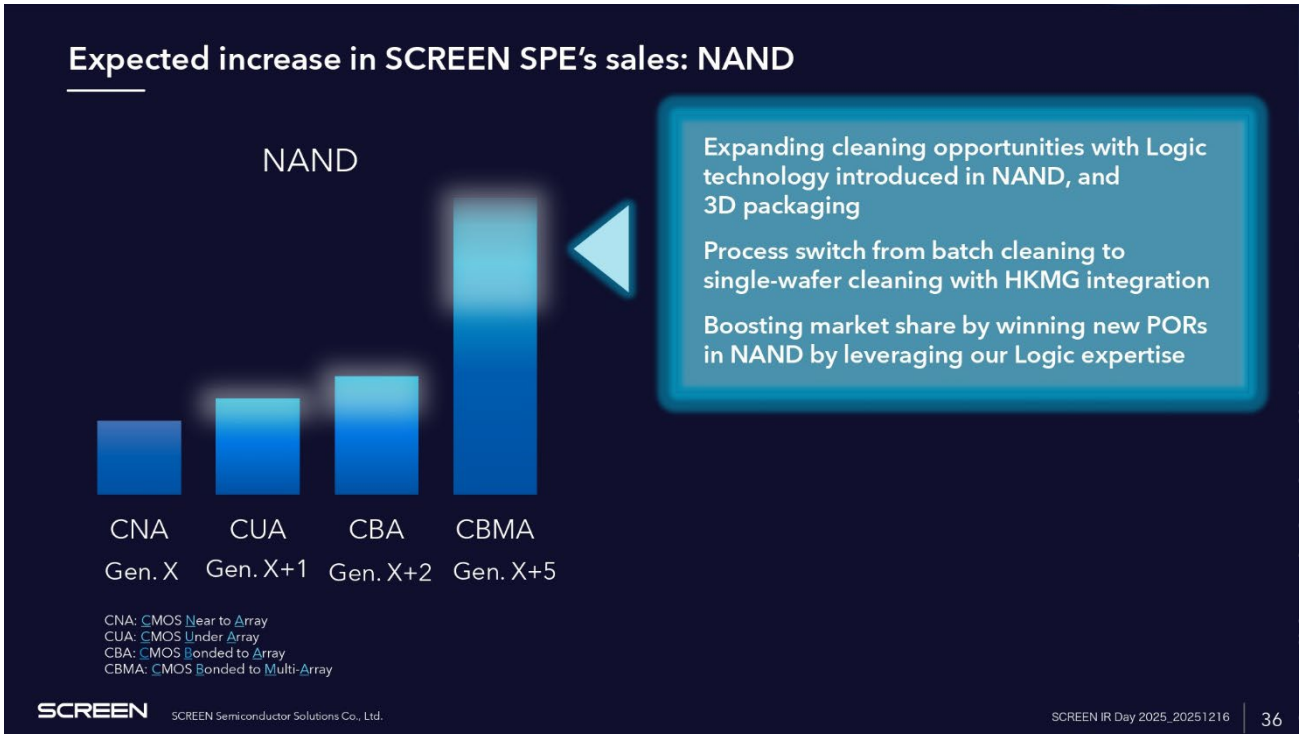
From here, we show three slides, not the number of process steps, but an image-based view of how our sales are trending.

The first is Logic. As you can see, from FinFET to Nanosheet and then toward sCFET, we aim to increase sales by adding value through refining our cleaning technologies to address these new Logic structures and new materials.

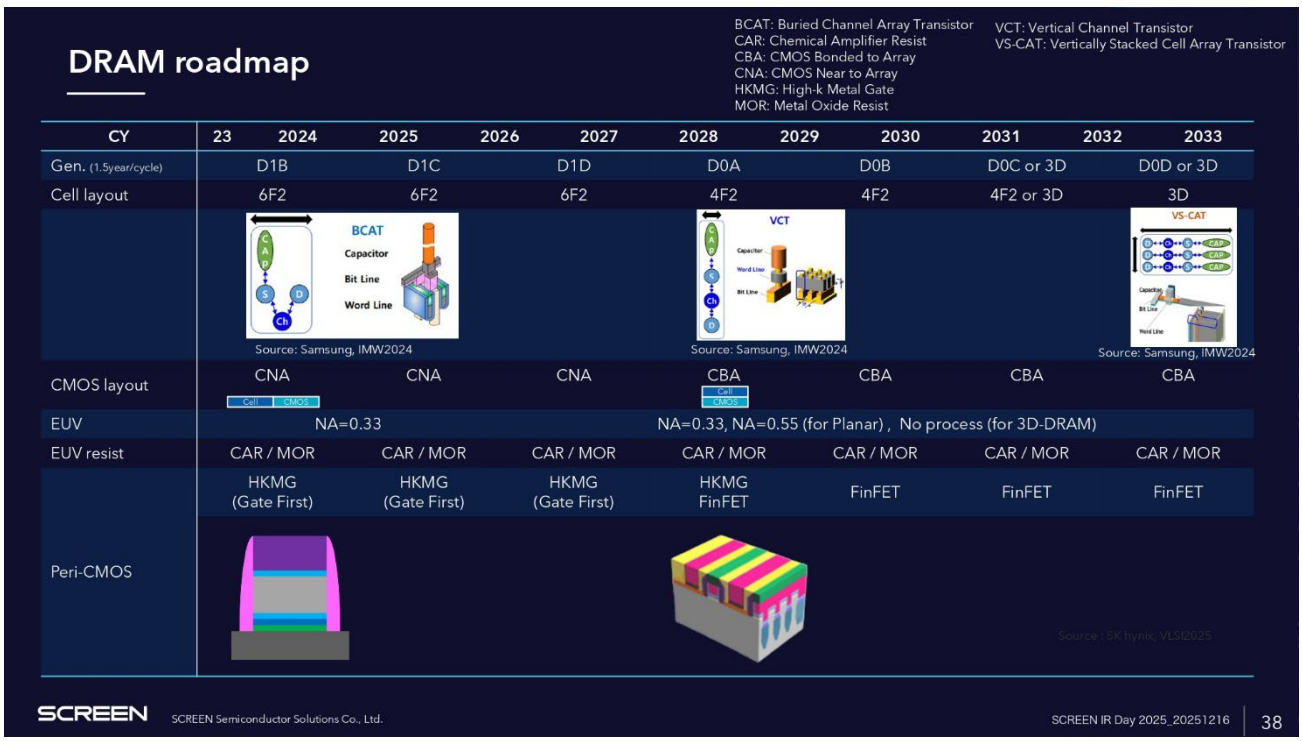


The same can be said for DRAM, and we expect it to grow not only in terms of the number of process steps but also on a value basis. The reason for this, which will come up again later, is that as Logic technologies are

applied to DRAM, we will leverage the Logic technologies and know-how we possess as our strengths and connect them to added value in these areas.



For NAND as well, in addition to the increase in cleaning opportunities as with DRAM, we see it growing significantly on a value basis by taking the application of past Logic technologies as a positive factor and adding value in that area.



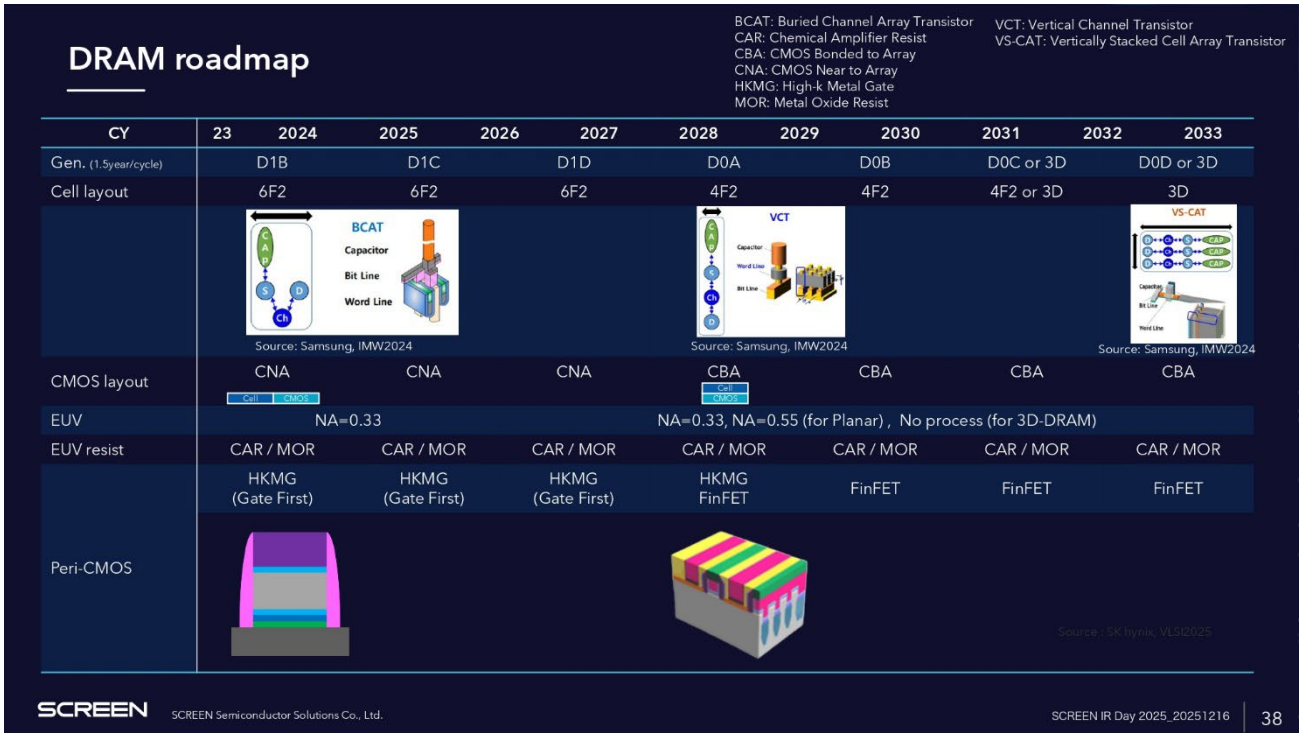
From here, I will briefly explain the roadmaps for various devices in the same way using three slides.

First, Logic. Logic starts with FinFET, then Nanosheet, then backside contact, and finally CFET.

In terms of major transition points for Logic, the EUV area shown around A16/A14 is the key point. We expect this to be the area where High NA EUV will be applied.

In addition, we anticipate that the type of resist used for High NA will shift to a metal oxide base.

Those are the major transition points for Logic, and I would like to touch on them a bit in a later slide.

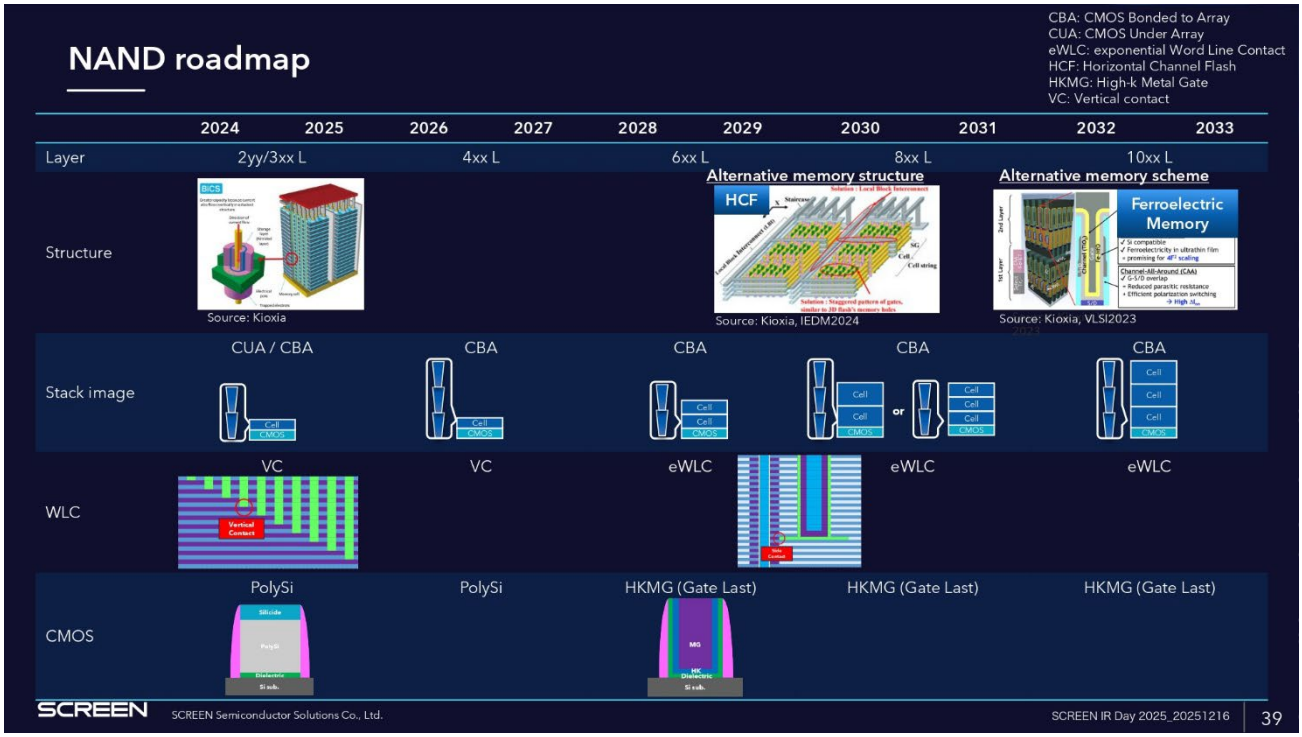


Next, let us look at DRAM. As mentioned earlier, for DRAM, the major transition point from a structural perspective is the transition from 6F2 to 4F2. In addition, with the move to 4F2, we expect a bonding process between the cell and CMOS to be introduced.

Beyond that, in the case of DRAM, studies are also being conducted on 3D DRAM, or horizontal DRAM, so this area is likely to be a major transition point.

In addition, as with Logic, we assume that High NA EUV will be adopted at one point, but as it progresses toward 3D DRAM, as shown further ahead, scaling will be selective, so we expect that some processes will become unnecessary for a time.

In addition, what is written at the bottom is the peripheral circuitry. For the peripheral circuitry, which is the part other than the memory cell, we expect major changes. In addition to the consideration of High-k Metal Gate, where Logic technology is already being deployed, we assume that FinFET technology will also be applied here.



Finally, NAND. For NAND as well, the number of stacked layers will continue to increase, and the discussion is that it will be stacked vertically. While stacking vertically, it will also follow the basic approach to building the structure, which is bonding the cell and CMOS, while increasing the number of cell layers to be stacked. Although it is not written here, there may also be the possibility that the number of CMOS layers increases.

Another point is that the method of making contact to the word line, which has been a feature of NAND, changes from so-called vertical contact to exponential word line contact, which will come up later. This change in the manufacturing approach is a major transition point for cleaning.

Finally, as with DRAM, the peripheral circuitry in NAND will also change, and we assume that the application of Logic technologies will progress.

Single-wafer cleaning for evolving DRAM and NAND processes

- Combining wafer cleaning and wet etching expertise, accommodating a range of device architecture, production, and processes, built over a half century.
- Accommodates wide-ranged evaluation during the development phase and smooth narrowing during the large-scale production phase.

Proven track records

- No.1 market share in single-wafer cleaning
- Supporting advanced Logic miniaturization
- Driving improvements in device yield

Features

- Multi-process chambers for loading several types of chemicals
- Acid, alkali, and organic chemicals can be loaded at the same time
- Allows to reclaim and reuse several types of chemicals
- Flexible chemical combinations possible with DDI*

*DDI: Dynamic Direct Injection

Process applications

- HF, APM, HPM, etc. (mainly for particle removal)
  - ✓ Pre-deposition clean, post-deposition/dry clean
- SPM (mainly for resist, organic residue, and slurry removal)
  - ✓ Resist removal
  - ✓ Post-process clean (DRY, CMP)
- Wet etching (mainly for processing)
  - ✓ Metal etch
  - ✓ Oxide film etch
  - ✓ Si etch

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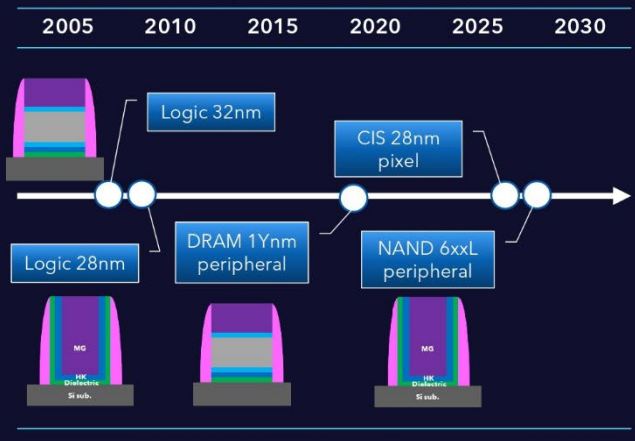
We are thinking of further increasing added value through our technologies in the areas where the Logic technologies I have just explained are being applied to DRAM and NAND.

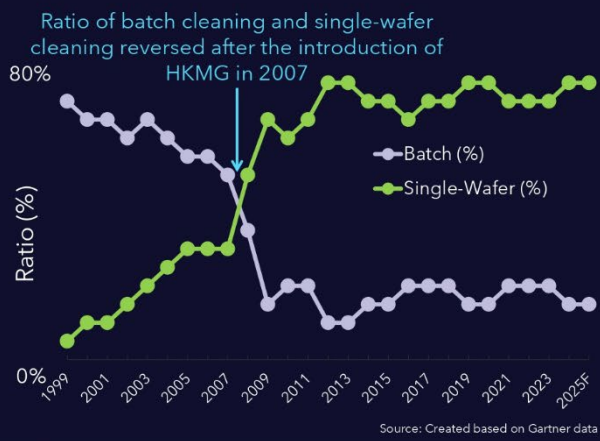
These are our technologies backed by both performance track records and functionality, so by leveraging technologies that can be applied across a wide range of process applications, we aim to steadily advance penetration into future DRAM and NAND processes.

Single-wafer cleaning more in demand with HKMG integration

HKMG: High-k Metal Gate

- HKMG-CMOS is increasingly adopted to accommodate the need for high-speed, energy-saving devices, in step with the AI revolution.
- Demand for single-wafer wet cleaning will increase further.





Source: Created based on Gartner data

Single-wafer wet cleaning are better suited to prevent cross contamination.

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As one example, I will introduce our own case regarding what changes occurred around 2007, when High-k Metal Gate was introduced.

To explain simply, using the graph on the right, this plots the ratio of our single-wafer cleaning and batch cleaning. Around 2007, there was a turning point when batch, which had been holding the primary share, was overtaken by single-wafer.

This turning point was the introduction of High-k Metal Gate in Logic. Going forward, it will be rolled out not only in Logic but also, as mentioned earlier, in DRAM, NAND, and CIS. In existing processes, the batch ratio is somewhat higher for DRAM, NAND, and CIS, but we believe that the single-wafer ratio will also increase relatively for these devices.

This is a photo from the signing ceremony with IBM, which I mentioned earlier in connection with our joint R&D related to High NA EUV. This is a major part of ATCA's activities, as also raised in the earlier question, and we will strongly promote joint R&D with IBM going forward.

Off-shore R&D base, "ATCA," established in New York

Press release published December 16, 2025: *SCREEN to establish an R&D center in Albany, New York for semiconductor production processes*

ATCA will be located within Albany NanoTech Complex, the state-of-the-art semiconductor facility operated by NY Creates (NYCR).

It will be using NYCR's clean room and other infrastructure to pursue solo research as well as joint research with global partners.

We will aim to increase our presence in wet cleans as well as thermal processing and advanced packaging.

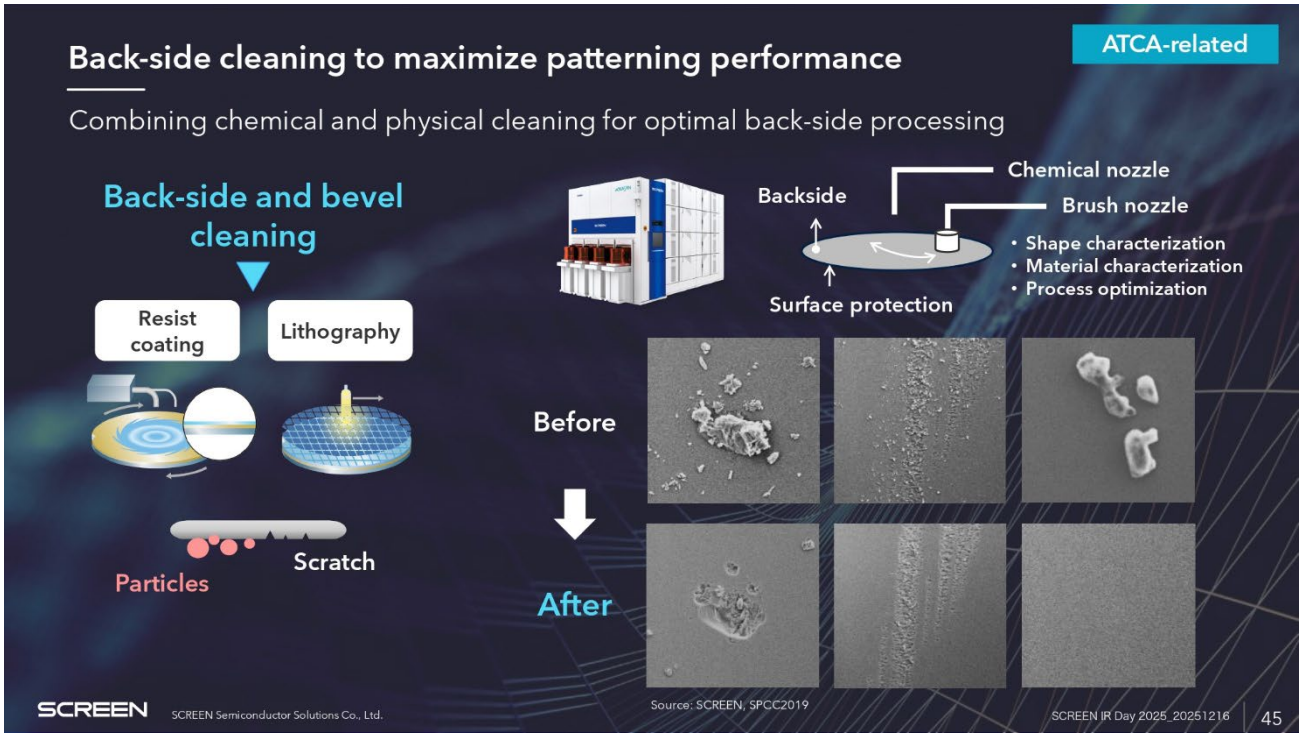
Specifically regarding ATCA's activities, first, we announced today that we have established a base. Here, we will conduct future R&D in fields not limited to wet cleaning but also including thermal processing and advanced packaging, and we aim to improve profitability and competitiveness and strengthen them across a wide range of fields.

Back-side and bevel cleaning: Growing importance in the EUV process flow

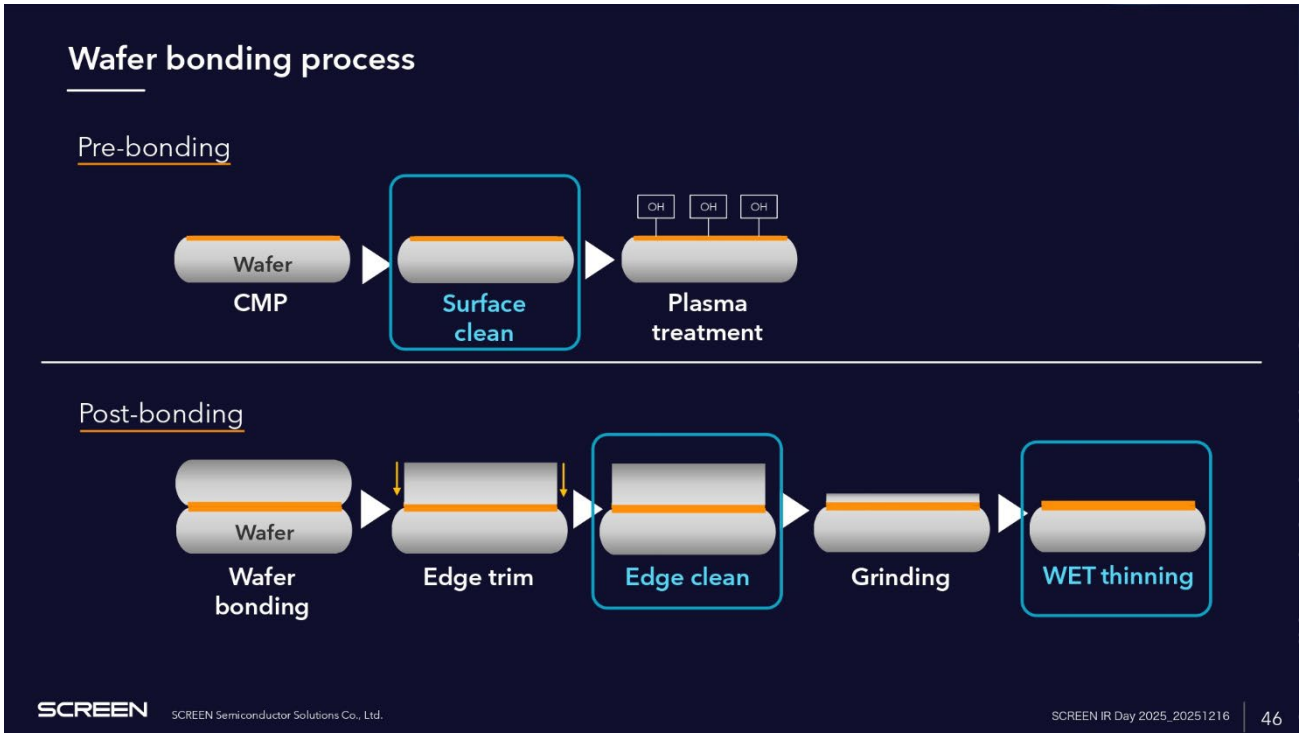
This is about why we are jointly developing technologies with IBM for the EUV process. Here, I have drawn a simple diagram of the process flow around the EUV process, moving from left to right.

In this process, what happens from actually coating the High NA EUV resist to development is as follows. First, regardless of the resistance, particles and scratches remain on the backside of the wafer, and it is known that if these are not properly controlled, they affect patterning on the front side, particularly the fine patterns that use EUV and High NA. Backside treatment is therefore essential.

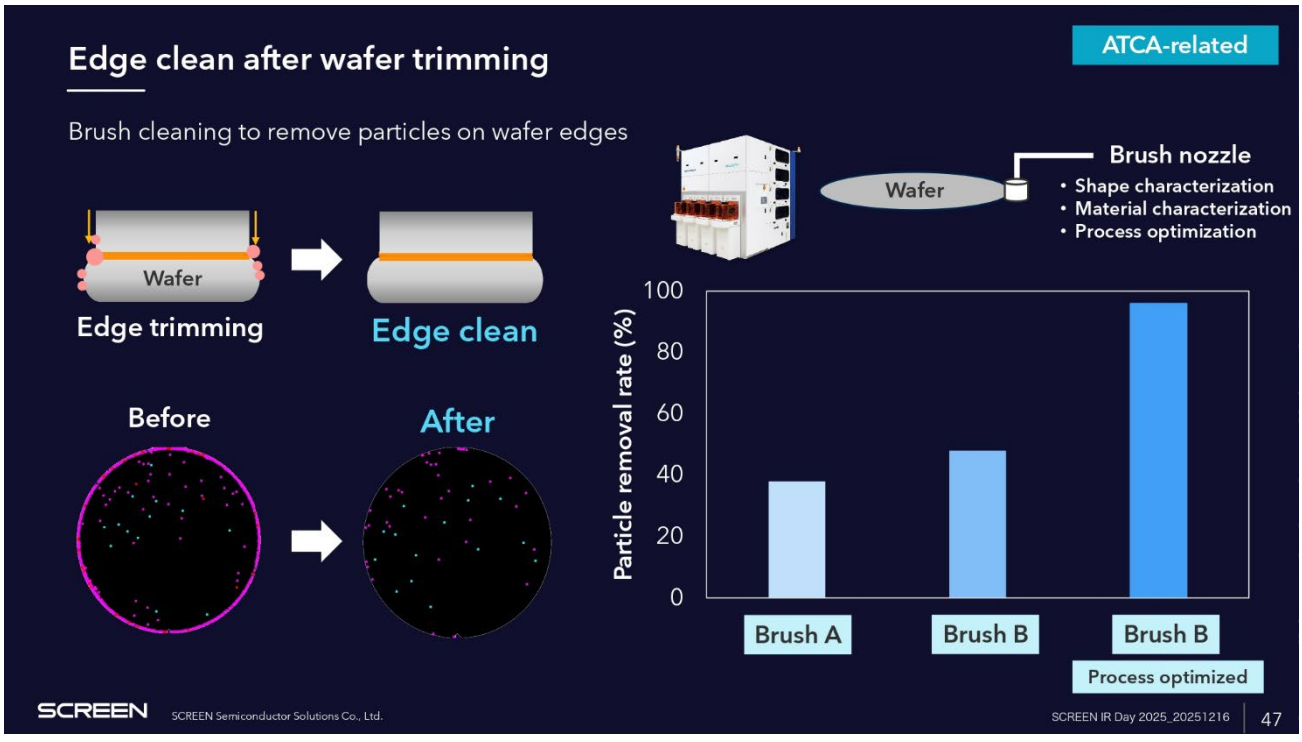
In addition, if we use a resist that contains metal oxide, it becomes necessary to properly control the metal contamination adhering around the wafer, so backside treatment and removal of metal contamination at the backside level are key.



We already have solutions that can address these issues. The key point is the combination of chemical and brush cleaning. We can optimize the process through a right combination of chemicals and brushes. We will leverage this to solidify our advantages for High NA EUV through joint initiative with IBM.



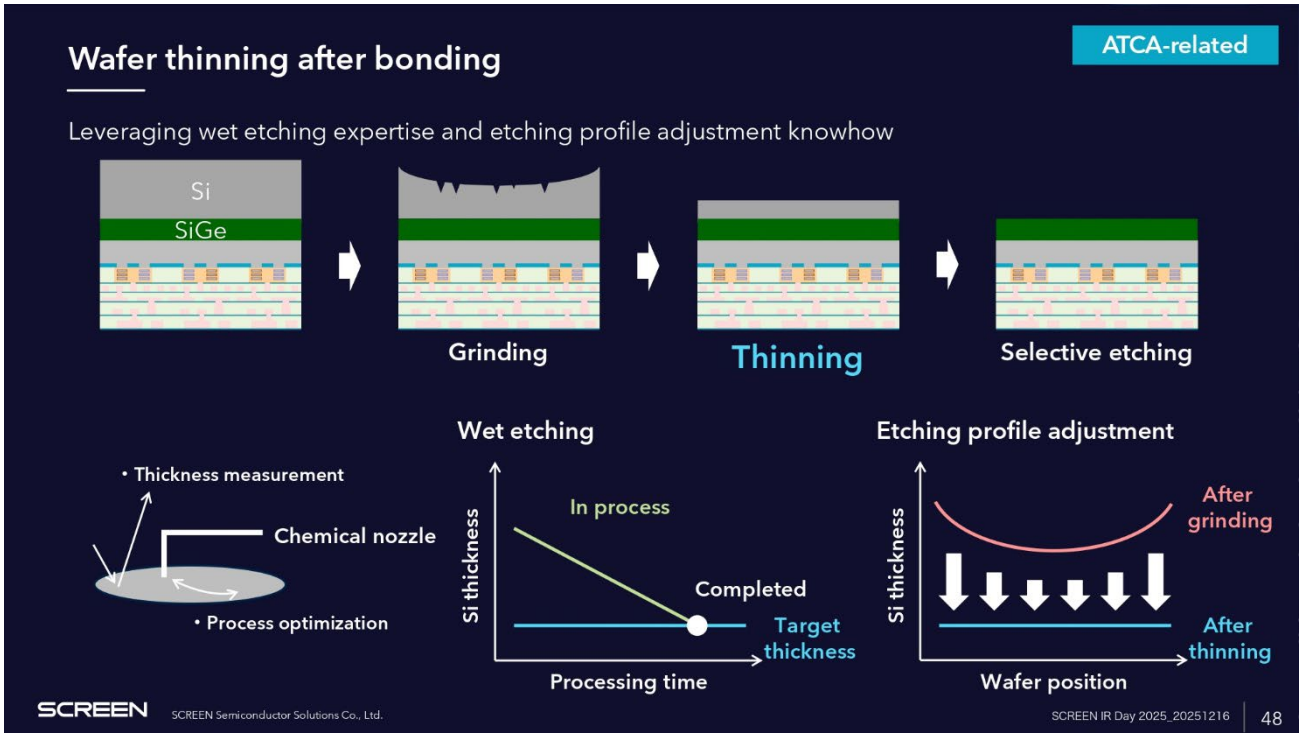
In addition, on a slightly different note, regarding where cleaning plays an active role in the wafer bonding process, this is something we also mentioned at the previous IR Day. One area is pre-bonding, such as cleaning prior to hybrid bonding. Post-bonding includes cleaning after edge trim, as well as cleaning during the step where polishing is performed. Finally, wet thinning is needed to complete the process.



First, this is cleaning after wafer trimming. After wafer trimming, a considerable amount of silicon debris and the like adheres to the edge side. When we measure it with an inspection tool, what appears purple is the signal indicating that foreign matter is present. Particles are densely attached around the wafer's outer periphery.

When we use our cleaning system, we can cleanly remove the particles attached around the periphery.

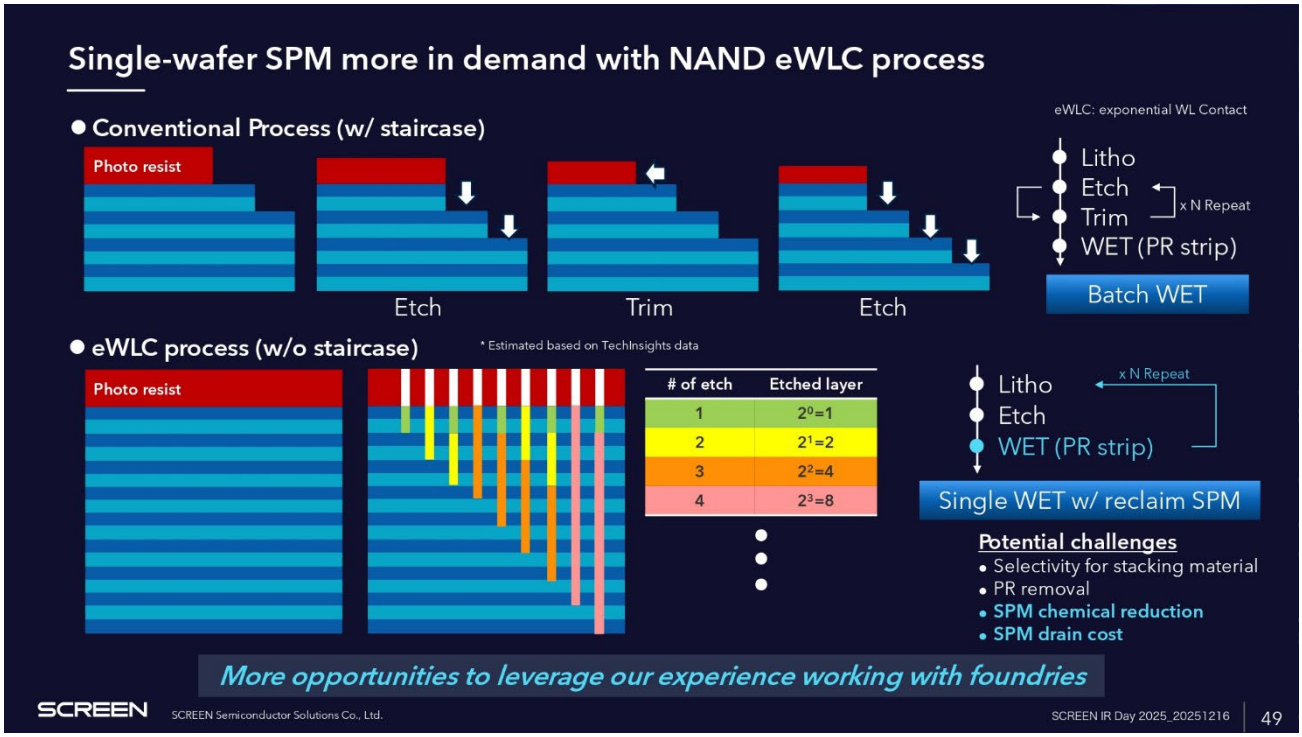
This does not simply end with the conclusion that they can be removed because there is know-how in how they are removed. We perform cleaning while applying the brush to the wafer, but this involves what brush shape is used—what is optimal and what the material characteristics are. It also involves how the brush is applied. Process optimization is also very important, and this graph shows the comparison. The vertical axis is the particle removal rate. It is best to reach 100%, and I think you can see that this removal rate approaches 100% by changing the brush and changing the process.



Next is wafer thinning after bonding. As for bonding, this shows an example of backside contact. After forming the device side, we flip it over and remove the silicon on the backside, then remove the top-layer silicon and gels as well, and ultimately want to access this active layer, but after polishing, the wafer comes to the wet process with the polishing tendencies remaining, such as film thickness variations and polishing scratches.

One of the features of our equipment is a function that enables the continuous monitoring of wafer film thickness inside the chamber, and it also has a function to adjust the optimum etching recipe based on the film thickness distribution.

This enables us to stop the process when the silicon film thickness reaches the target, regardless of the incoming film thickness, and it also enables us to align incoming wafer film thicknesses that have variations and then send them to the next process.



Finally, I will introduce NAND exponential word line contact. Conventionally, this process repeats edge trim while creating a staircase-shaped pattern.

The feature here is that edge trim is repeated at the points indicated by the arrows, and after it is completed, wet processing comes all at once at the end, so wet processing appears only once.

In contrast, the next process being considered is this exponential process. What it is, in short, is a method that enables access to each layer of the vertically stacked layers through a combination of etching repeated in powers of two, namely, 1 time, 2 times, 4 times, 8 times, 16 times, and 32 times.

In that case, lithography, etching, and wet processing become one pair and are repeated, so the number of wet processes increases in line with the number of repetitions.

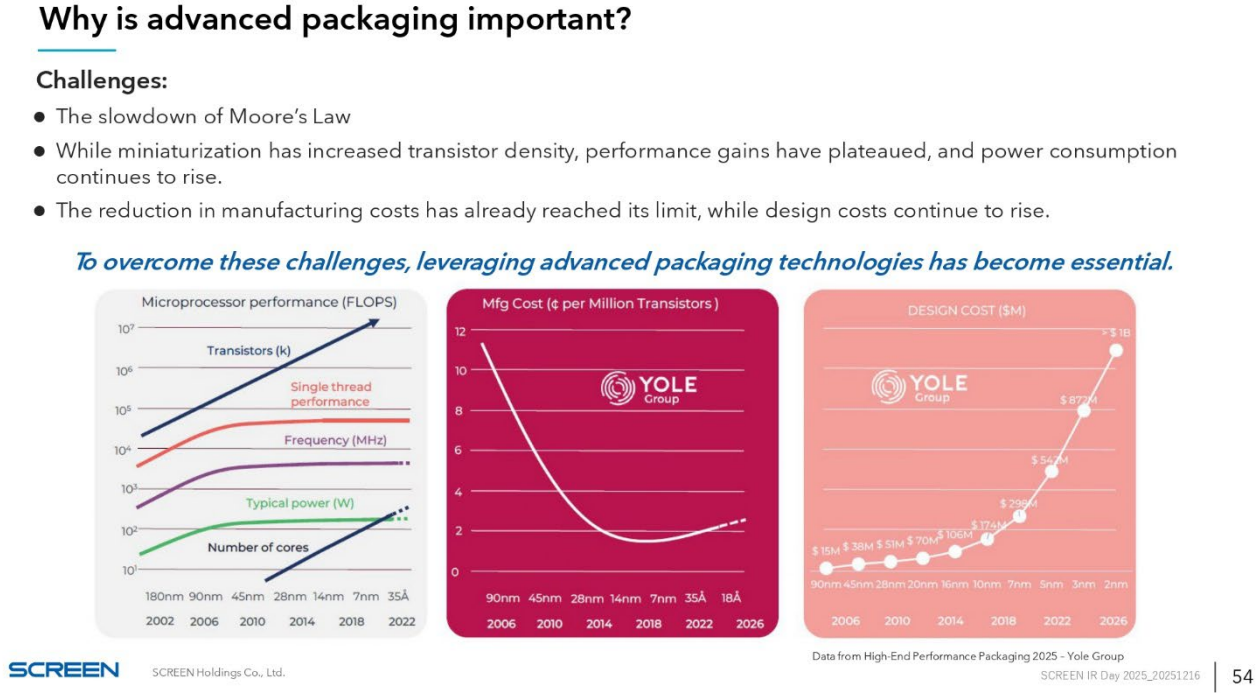
One thing we anticipate here is that what has been performed as batch processing up to now will likely transition to single-wafer processing. As that happens, we believe that our know-how and technological assets for Logic SPM can be deployed effectively.

Lastly, in summary, for each device, we would like to aim for further growth in cleaning by leveraging our competitive advantages. Specifically, we believe that the keywords of new materials and new architectures will lead to the next processes.

That is all. Thank you very much.

Moderator: Thank you, Managing Director Takahashi. Next, General Manager Nishimura will explain the future outlook for advanced packaging.

General Manager Nishimura, if you would please.



Nishimura: Hello, everyone. I am Nishimura from the Advanced Package Department. Thank you.

First, regarding our initiatives in advanced packaging and the future, I would like to explain what we are focusing and working on.

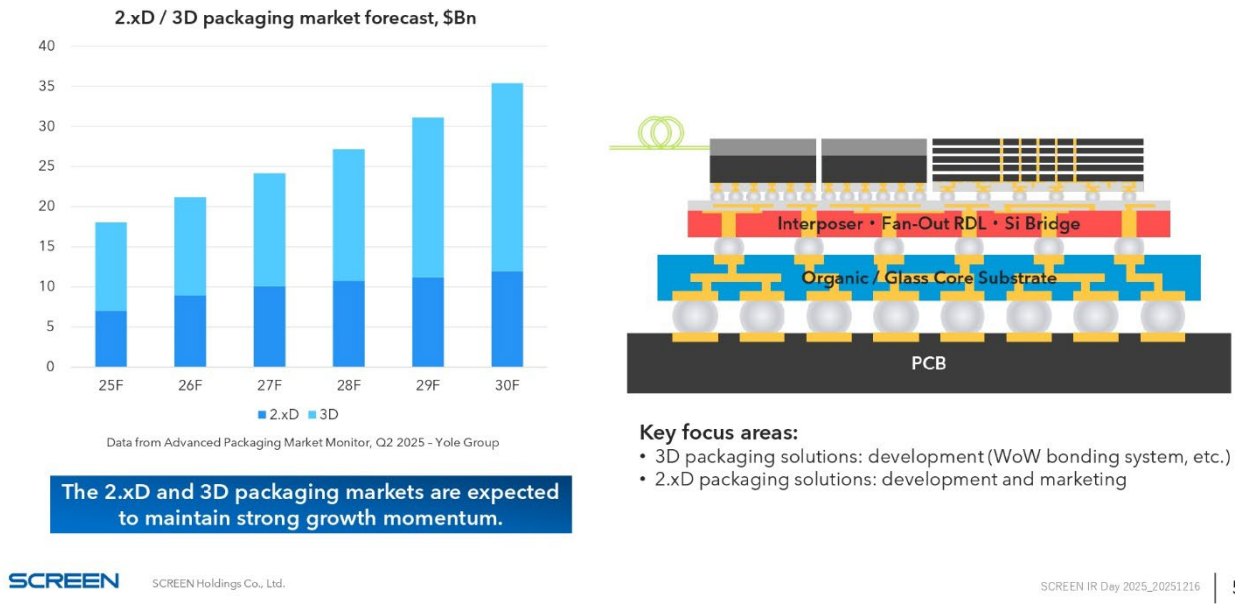
Before that, let me start with why advanced packaging is necessary. Many people have already discussed this in many places, so I do not think it is necessary to provide a detailed explanation here.

AI, particularly the spread of generative AI, has significantly raised the performance requirements for semiconductor chips. In particular, performance is required in areas with larger capacity, higher speed, and lower power consumption.

In the past, these capabilities were achieved through the scaling of semiconductor chips. Recently, however, chips alone are no longer sufficient. In other words, these performance requirements must be achieved in the context of electronic components, or the overall system, including the package substrate on which the chip is installed and mounted, the underlying substrate, and the overall system. In that sense, the use of advanced packaging has become extremely essential.

Specifically, the challenges that are driving this include the slowdown in scaling. While scaling naturally increases the number of transistors, there is the issue of power consumption and the resulting increase must be addressed.

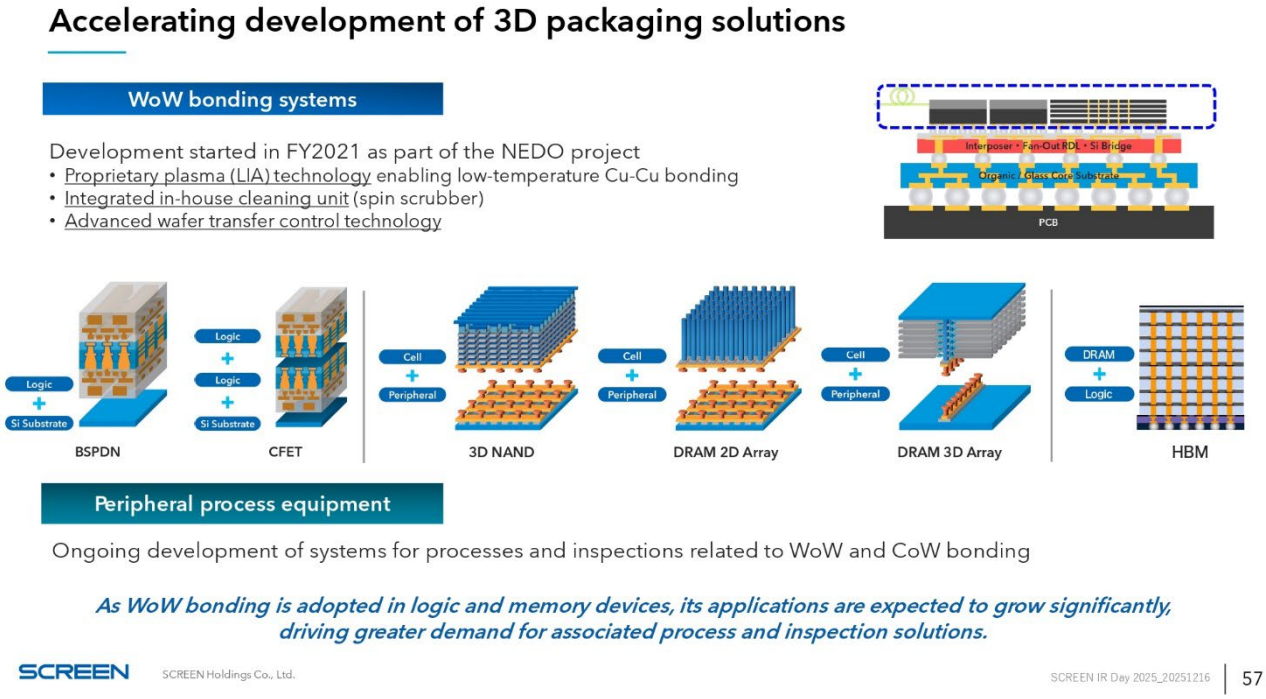
In addition, manufacturing costs, as shown here, are increasing as the structure becomes more complex. Design costs are also increasing, and advanced packaging is necessary to solve these issues.



We are focusing on the areas for advanced packaging shown on the right. This is a general illustration, but we are considering two segments.

One is for 3D. I will explain the details later, but this refers to the chip area, specifically chip stacking. As Mr. Takahashi also briefly explained earlier, this is the area where bonding is performed for silicon wafers. The other is the package referred to as 2.xD below. We are conducting various activities with a focus on these two areas.

We also expect continued high growth in the market for 2.XD and 3D, so by addressing these areas, we hope to increase our earnings as well.



I will explain the details of each initiative.

This is our 3D solution. As I mentioned earlier, we are working on stacking in the upper chip area.

In terms of applications, as Mr. Takahashi also mentioned earlier, wafer stacking originally began with backside illumination for CMOS image sensors. However, now, wafer stacking has been adopted for Logic and memory. As for memory, what is currently drawing significant attention is high-bandwidth memory (HBM). This is also an area where wafer stacking has been adopted.

In this context, in 2021, we began R&D with support from a NEDO project. As Mr. Yasui also mentioned earlier, based on our core technologies, namely, surface activation and cleaning technologies, as well as underlying technologies, such as alignment, which is required to position wafers, and mechanical engineering that integrate the entire process, we have independently developed a wafer bonding system.

That is one point.

Another point is that regarding wafer bonding, we are also advancing R&D in the peripheral areas. While we are not yet at the stage where we can explain specifically what this involves here, this includes the processing of the edge area after wafer bonding, as well as inspection systems for conducting various inspections after bonding.

Since we have not yet reached the productization level, I will refrain from going into detail here.

Acquisition of an R&D business in wafer bonding from Nikon

(effective on September 30, announced October 31, 2025)

SCREEN
SCREEN Holdings

News Release
October 31, 2025

Acquisition of an R&D business in wafer bonding from Nikon

SCREEN Holdings Co., Ltd. (SCREEN HD, President & CEO: Masato Goto) hereby announces the acquisition of an R&D business in wafer bonding from Nikon Corporation (Nikon; headquarters: Tokyo; Representative Director and Chairman: Toshikazu Umatate), effective on September 30.

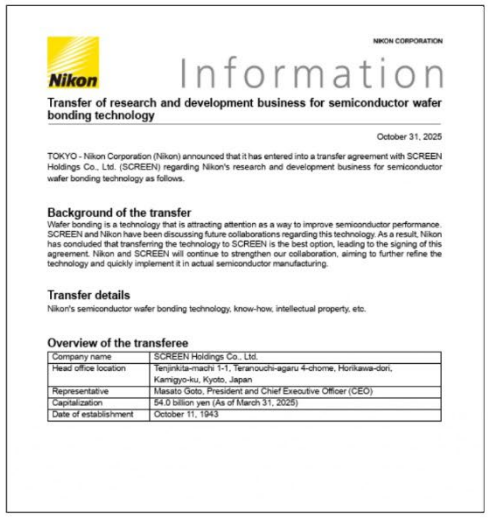
In the semiconductor advanced packaging field, expectations are rising for more high-precision wafer bonding to support the increasing demand for footprint- and energy-saving devices. Positioning advanced packaging as a focus field, in addition to the sales of direct imaging systems and coater/dryer systems, we are working on the development and roll-out of low-temperature wafer bonding. The latest acquisition will allow us to combine Nikon's ultra-high-precision bonding technology with our proprietary technology as we seek to lead the world in bonding technology and establish a presence in this field.

Under the current medium-term management plan, Value Up Further 2026, covering the three fiscal years ending March 2027, SCREEN has been investing intensively for growth. In particular, we focus on advanced packaging as a new business field with a high growth potential, leading to the latest acquisition. The acquisition has already been reflected in the business plan for this fiscal year and therefore will not impact our earnings forecasts.

SCREEN will continue serving diverse client needs in the semiconductor packaging industry and contribute to its further development.

Overview of the acquisition

1. Acquired business	Nikon's R&D business in wafer bonding
2. Acquired from	NIKON CORPORATION Headquarters: 1-5-20 Nishioi, Shinagawa-ku, Tokyo, Japan Representative Director and Chairman: Toshikazu Umatate Capitalization: JPY 65,476 million (as of March 31, 2025) Established: July 25, 1917
3. Date of agreement	August 14, 2025
4. Date of acquisition	September 30, 2025



NIKON CORPORATION

Nikon

Information

Transfer of research and development business for semiconductor wafer bonding technology

October 31, 2025

TOKYO - Nikon Corporation (Nikon) announced that it has entered into a transfer agreement with SCREEN Holdings Co., Ltd. (SCREEN) regarding Nikon's research and development business for semiconductor wafer bonding technology as follows.

Background of the transfer

Wafer bonding is a technology that is attracting attention as a way to improve semiconductor performance. SCREEN and Nikon have been discussing future collaborations regarding this technology. As a result, Nikon has concluded that transferring the technology to SCREEN is the best option, leading to the signing of this agreement. Nikon and SCREEN will continue to strengthen our collaboration, aiming to further refine the technology and quickly implement it in actual semiconductor manufacturing.

Transfer details

Nikon's semiconductor wafer bonding technology, know-how, intellectual property, etc.

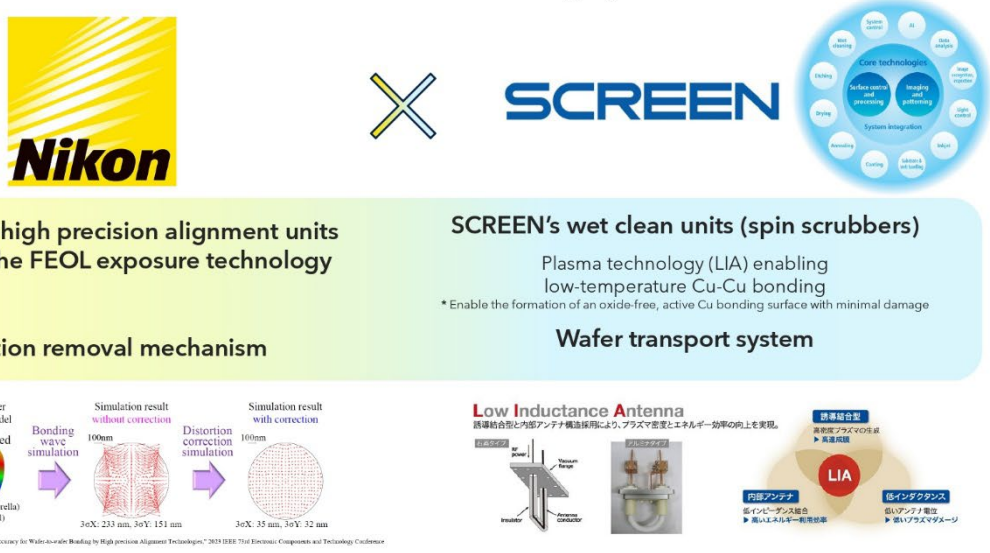
Overview of the transferee

Company name	SCREEN Holdings Co., Ltd.
Head office location	Tenjinkita-machi 1-1, Teranouchi-agaru 4-chome, Horikawa-dori, Kamigyo-ku, Kyoto, Japan
Representative	Masato Goto, President and Chief Executive Officer (CEO)
Capitalization	54.0 billion yen (As of March 31, 2025)
Date of establishment	October 11, 1943

Source: News releases of the respective companies.

In that context, on September 30, we received a business transfer from Nikon, which has been developing wafer bonding technology for around 20 years, and we are now in a situation where we will proceed with development aimed at further improving precision.

Advantages of our wafer-on-wafer (WoW) bonding system



Nikon × SCREEN

Core technologies: Surface control and processing; Imaging and patterning; System integration

Nikon's ultra-high precision alignment units leveraging the FEOL exposure technology

Distortion removal mechanism

SCREEN's wet clean units (spin scrubbers)

Plasma technology (LIA) enabling low-temperature Cu-Cu bonding

* Enable the formation of an oxide-free, active Cu bonding surface with minimal damage

Wafer transport system

Source: H. Mitsuishi et al., "50 nm Overlay Accuracy for Wafer-to-wafer Bonding by High precision Alignment Technologies," 2023 IEEE 73rd Electronic Components and Technology Conference

By combining both technologies, we are positioned to address the evolving market demands for WoW bonding systems, which are expected to become increasingly advanced and complex.

Using this Nikon technology, what can we do? First, on the right side, these are the technologies that SCREEN has independently developed. A cleaning unit and unique plasma technology to activate the surface. This enables copper to adhere at low temperatures. We have already presented this at academic conferences, and it is a technology that uses our proprietary plasma LIA to form the high-density bonding surface with low damage. In addition, we are developing technology to transport wafers or build an equipment system.

Our technologies at SCREEN, and Nikon's ultra-high-precision alignment technology, stage technology, and distortion correction technology derived from exposure tools, given that Nikon has long worked on exposure tools. This distortion correction technology has become extremely important in recent years.

Previously, the focus was on how to optimize alignment for copper-to-copper bonding, and at what pitch and how much it could be increased. However, as the applications I mentioned earlier expand, how to bond wafers without distortion has become a key process.

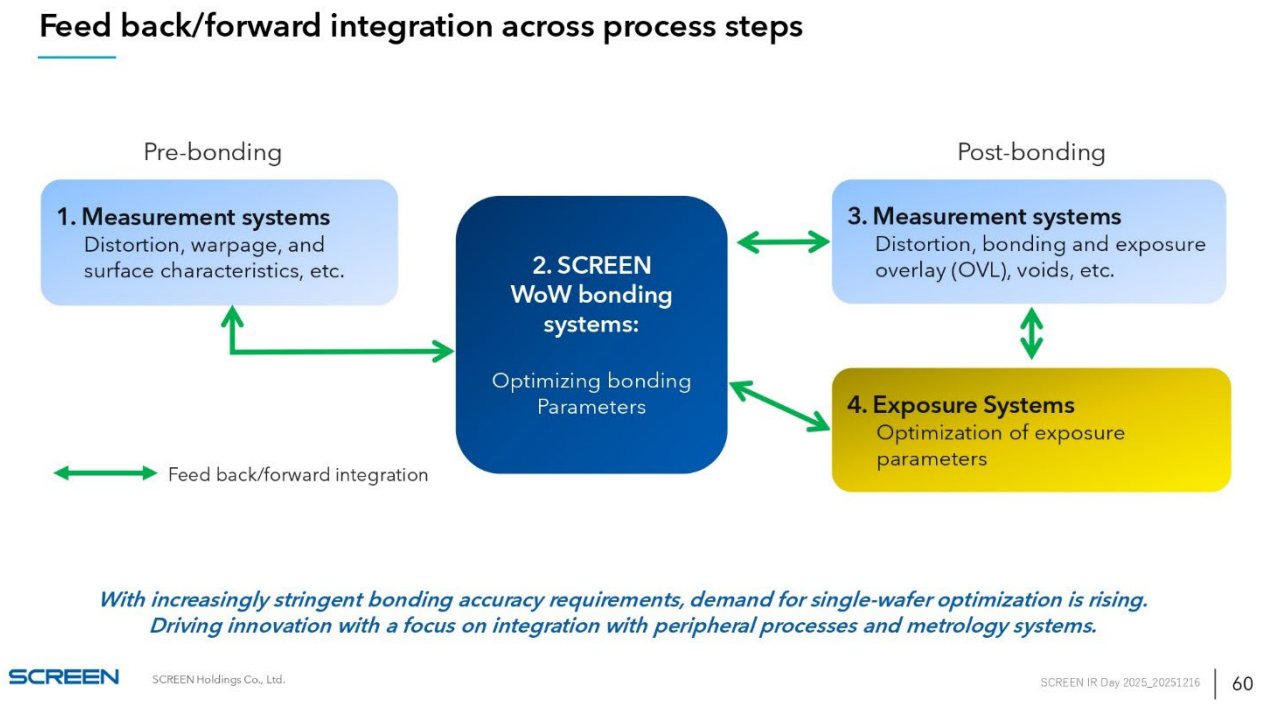
To be specific, this is content that Nikon presented at ECTC. It is publicly announced technology, so I will explain it.

Even if you bond wafers with flat surfaces, they become distorted due to crystal/lattice stress, in other words, because the directions in which they elongate are different. In addition, this assumes NAND in particular, it is saddle-shaped. In other words, it is a wafer with an asymmetrical warp. If you try to bond this, it becomes extremely distorted.

This is a simulation result, so it was not actually bonded, but when Nikon runs it through its simulation, bonding a wafer warped by around 250 microns results in distortion on the surface. Distortion around 200 nm occurs. Using correction technology, it can be reduced to around 30 nanometers. It is this type of technology. Distortion correction is performed using this type of technology.

In addition, our LIA adopts a plasma method with this type of shape, called a low-inductance antenna. By adjusting the gas supplied here, it has the feature that copper can now be at a low temperature of 250 degrees or below.

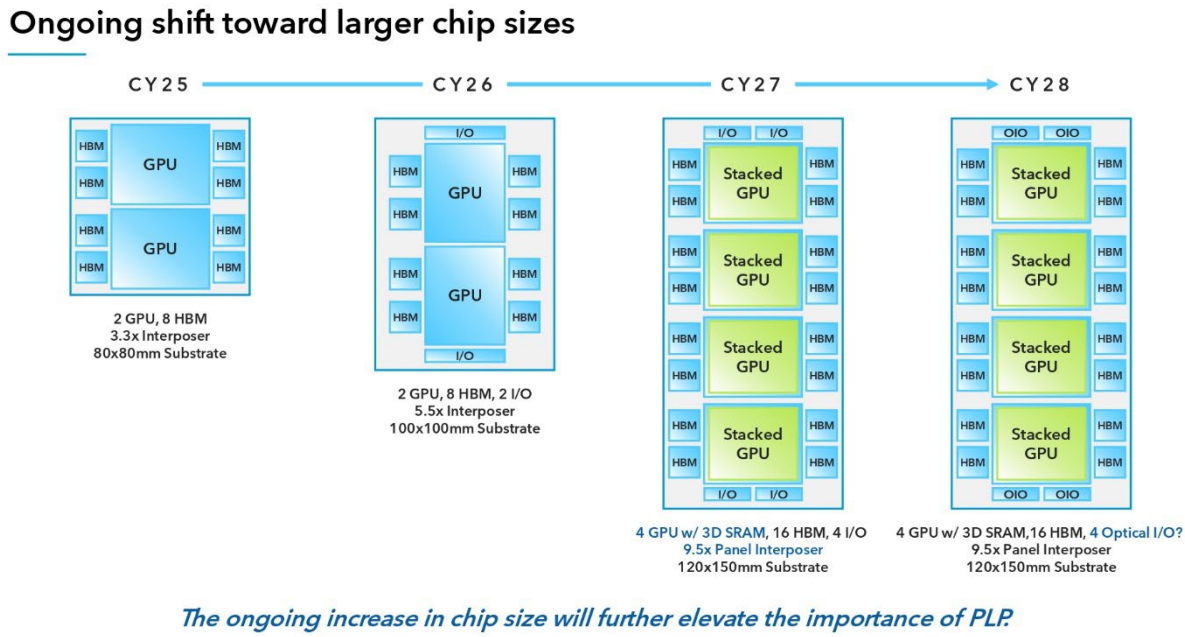
By combining these two and making it into a unified system, we intend to accommodate market needs for wafer bonding systems that will become increasingly sophisticated and complex going forward.



Lastly, in this case, regarding the competition with Nikon on exposure. We have a bonder. We also have an overall feedback and feedforward system where distortion after bonding is measured, and corrections are then applied on the exposure tool side.

I understand that the degree of wafer distortion, especially in case of NAND, differ by each wafer. First, before bonding, each wafer is measured in advance. A simulation is run to determine what kind of distortion will occur when they are bonded. Then, a feedforward linkage is used so that the bonder side applies corrections so that they do not become distorted when bonded. By doing so, we are also considering further improving alignment accuracy and enhancing distortion performance with high precision.

That is our initiatives in the 3D domain.



Next, I would like to explain 2.XD, the area referred to as packaging. As you all likely know, package sizes are getting larger and larger, and up to now, in many cases, interposers have been made with silicon.

However, at this size, only about five interposers can be produced from a 300 mm silicon wafer, and the importance of panels is increasing rapidly.

In that context, we have taken the lead by releasing a direct maskless exposure system for panels, as Mr. Goto also mentioned earlier, LeVina, and a slit coater, "Lemotia," which applies resist to square panels. We have released these two products.

Regarding size, LeVina supports a maximum size of 620 to 650 mm. There are two models. One is a system that can achieve 5 microns by 5 microns L/S. The other is a system that can achieve 2 microns by 2 microns L/S. We have already developed and are selling these two models.

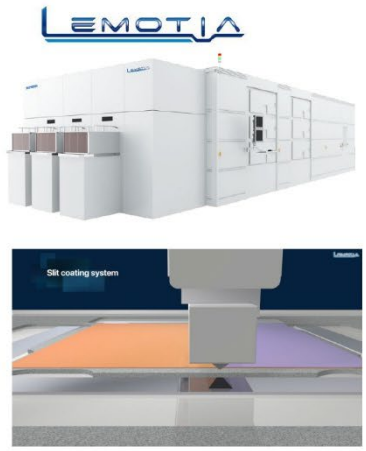
Regarding Lemotia, it has been on the market about two years. We released a slit coater applicable to large panel sizes of 600 mm x 600 mm. Recently, on December 10, recently, we released a different, though similar, shrunk system specialized for 310 mm x 310 mm and 300 mm x 300 mm, focusing on smaller sizes, and we have a lineup of systems that can be applied to various sizes.

First, as a demonstration area for panels, we have constructed a line where lithography can be performed in an integrated manner at S^3-6, which was completed recently. We are currently installing equipment as needed, and we plan to complete it to a certain extent within this fiscal year and proceed so that we can conduct customer demonstrations starting in the next fiscal year.

Spin coater vs slit coater: Comparison

	Spin Coating	Slit Coating
Consistency	Difficult to coat corner edge	Compliant with the PLP standard
Thick film coating	Difficult	Possible
EBR	Required & difficult (Due to warpage)	Not required
Low-pressure drying	Not required	Required
Chemical usage	Large amount	Small amount
Distortion adjustment	Required to develop	Already available
Panel size expandability	Required to develop	Proven in the FPD market

Note: Comparison based on SCREEN's in-house experiment.



Slit coater is better suited for panel coating due to consistency, less chemical use, and capability to adjusts panel distortion, accommodating the future expansion of panel size.

Originally, in wafer-level packaging, since we coat on round wafers, slit coating has been the default standard.

We actually performed spin coating for small sizes in display applications and spin coating on rectangular substrates. Since we have experience with that, this time we show a comparison between spin coating and slit coating.

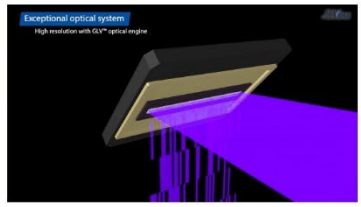
Basically, in terms of coating uniformity, chemical usage volume, substrate warpage prevention, and scalability in panel size, we believe slit coating is more suitable.

There is a video, please take a look.

As shown in this simple animation, we set the substrate, since it is warped, we hold and suction it down on all four sides, the nozzle comes out, and it places the chemical on the wafer. This allows uniform coating, whereas since spin coating involves spinning, it inevitably discards chemicals. Since it also adheres to the edges, EBR is always required. However, with a slit coater, those are not necessary, and chemical usage volume can also be reduced, so from SCREEN's perspective, we think it has a greater advantage.

Our exposure systems

Application	PLP/WLP	PLP	PLP	FCBGA/FCCSP/ MCM	FCBGA/MCP	FCCSP/MCM
Wavelength	375nmLD	375nmLD	405nmLD	405nmLD	Broad	Broad
Model	DW-3100	LeVina-i	LeVina-h	LUPIOS	Ledia Qs	Ledia 8F
Productivity						
Resolution (L/S)	≦ 1/1μm	2/2μm	5/5μm	8/8μm	10/10μm	12/12μm
Maximum Exposure Area	310 × 310 mm	620 × 650 mm	620 × 650 mm	546 × 635 mm	587 × 661 mm	610 × 661 mm
Overlay (Ave + 3σ)	0.5μm	2.0μm	3.5μm	3.5μm	5μm	5μm



LeVina and the DW series feature SCREEN's GLV™ optical engine

Expanding our product lineup further to address diversified exposure needs in advanced packaging.

SCREEN Holdings Co., Ltd. SCREEN IR Day 2025_20251216 | 65

Finally, the maskless exposure system. We call it direct imaging. SCREEN has maintained a wide lineup for a long time, particularly direct imaging systems for printed circuit boards.

The further to the left, the higher the precision. This is a direct imaging system specialized for 300 mm wafers for 310-by-310 rectangular formats, the recently released DW-3100 from SPE.

As direct imaging systems developed for advanced packaging, we have LeVina systems that support 2-micron L/S and 5-micron L/S. These are for large formats, targeting large panel sizes.

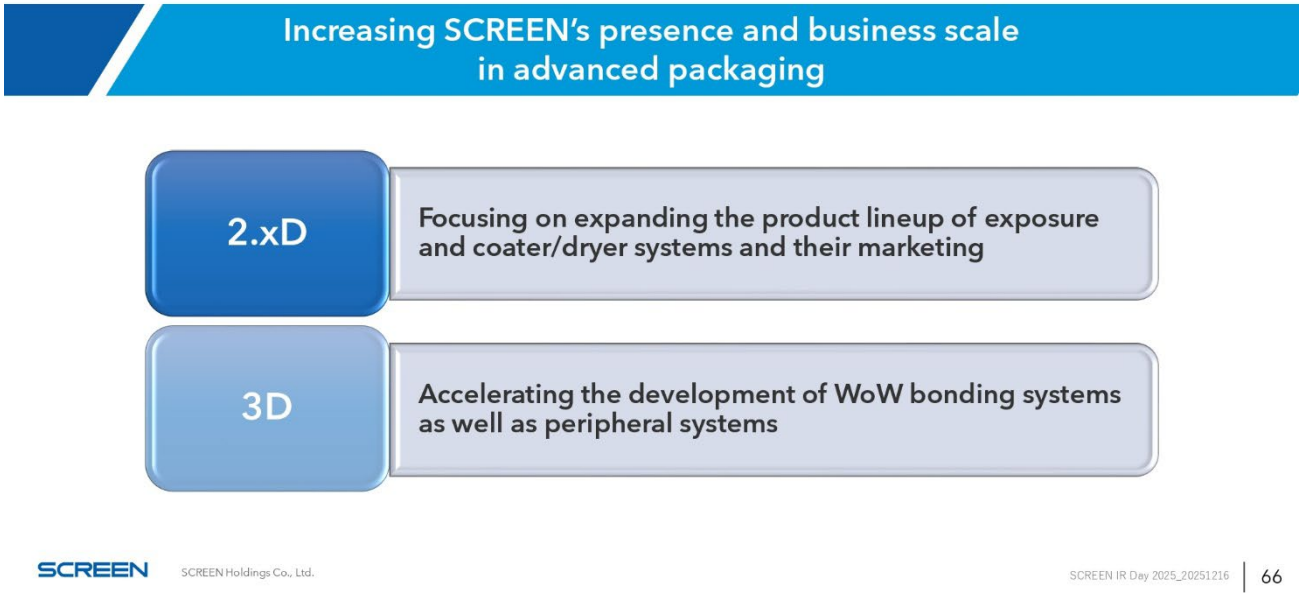
These are systems used in the advanced packaging area. For the drawing engine, we use SCREEN's proprietary GLV. Light emitted from the illuminator hits the substrate. The GLV has 8,172 ribbons, made internally. Light hits here, and by turning this on and off, a specified pattern can be drawn. We have been doing this using SCREEN's proprietary engine.

Now, these three models use GLV. For areas where L/S is strict and high precision is required, we use these GLV-mounted systems.

In addition, for printed circuit boards, we have a somewhat rougher direct imaging systems. They are marketed by PE.

As such, in the advanced packaging field, there are various requirements for these exposure tools, and we respond with a broad product lineup.

Summary



In summary, our advanced packaging business is focusing on the 3D and 2.xD areas.

For 2.xD, we have already developed and are manufacturing and selling exposure tools, slit coaters, and coater/dryer systems, and we believe that we will contribute to earnings by expanding the lineup and focusing on sales.

Regarding 3D, we are not yet selling it, but by accelerating the development of wafer-to-wafer bonding systems, peripheral systems for post-bonding, and inspection systems, we can contribute to SCREEN's earnings when the time comes.

That concludes my explanation. Thank you very much.

Moderator: Thank you, General Manager Nishimura.

Question & Answer

Moderator [M]: We will now move on to the Q&A session for the overall presentation. Due to time constraints, as I mentioned earlier, we would like to limit questions to two per person. Thank you for your cooperation.

Mr. Yoshioka, please.

Yoshioka [Q]: I am Yoshioka from Nomura Securities. I have two questions. One is regarding cleaning technology, and the other is regarding the overall presentation.

First, regarding cleaning technology. In terms of the slides, on pages 33 and 34, I believe you are showing, on the premise that there will be evolution in Logic going forward, how you will generate the number of process steps and sales.

What concerns me is that the increase in sales appears quite large compared to the increase in the number of process steps. As a result, I was looking at whether the unit price, for example, will rise. Specifically, are you seeing any areas where the unit price will rise going forward, such as through the introduction of new equipment? That is my first question.

Takahashi [A]: Thank you. While I cannot go so far as to introduce specific equipment under development, we are proceeding with the development of equipment that will provide future technical solutions for those devices, not limited to Logic, and since that will lead to improved added value, we assume that sales prices will inevitably rise as well.

Yoshioka [Q]: My second question is regarding the overall presentation, and it somewhat overlaps with a question that was asked in the first session regarding profit margin.

While margins have been improving recently, you indicated a direction of catching up to benchmarks in the SPE industry. From your current perspective, when comparing with other SPE companies, what factors are somewhat lowering and pushing down your profit margin?

There may be various factors, such as market share and costs, but could you please tell us again, your current understanding of what the company needs to catch up?

Goto [A]: I would like to explain.

I think there are various aspects to improving profit margin. First, in our manufacturing, there is still a room for improvement in how we control inventory and shorten lead times. Another point is that in our manufacturing, there are many areas where we are doing fairly labor-intensive processes.

That is because there are many areas that still rely heavily on people. Since factory utilization is influenced by people's time, within SPE, we will move forward with various initiatives to operate our cleanrooms 24 hours a day, by using robots and so on. In that sense, through such activities, production efficiency will improve.

As you know, people are becoming more expensive year after year, with wage increases and base pay increases, and also rising in line with higher prices. There is an upfront cost for introducing new facility, but there is also a mechanism where costs gradually decline through depreciation. This is just one example, but through various initiatives like these, we would like to enhance profitability.

Yoshioka [M]: Understood.

Moderator [M]: Thank you very much. Next, Mr. Nakamura, please.

Nakamura [Q]: Thank you. I am Nakamura from Goldman Sachs.

My first question is about the bonding equipment for wafer-on-wafer. I think that at present, your company is a latecomer relative to competitors in Japan and Europe. For this area, in a long term, what would be your company's differentiating factors? Also, could you tell us about the scale of the sales you aim for going forward, and things like that?

Takahashi [A]: Thank you. First, in terms of differentiation, as explained earlier, hybrid bonding and copper connection. By using our LIA technology here, the temperature for annealing after each anneal is such that copper adheres at 250 degrees or below.

At present, if you use ordinary plasma, it is difficult for it to adhere unless it is 350 degrees or higher. We can propose that point, and in particular, memory has strong requirements for low-temperature bonding, so we believe there may be a room to compete in such areas.

In addition, as explained earlier, the distortion correction that Nikon originally had. In this area, wafers with warpage, which NAND has in particular, can be bonded, with distortion at around the 50 nm level. These are two points for this distortion correction technology. Using these, although we are a latecomer, we can compete with these companies.

In addition, regarding earnings, or the volume, we aim for overall advanced packaging earnings at the mid-double-digit billion-yen level around 2030, so we hope that about 40% of that can be contributed by this bonding.

Nakamura [Q]: Do you mean the mid-double-digit billion-yen level with bonding plus direct imaging, correct?

Nishimura [A]: Yes, that is correct. We would like to aim for around the middle.

Nakamura [Q]: Understood, thank you.

My second question is about the breakdown of the JPY80 billion in strategic investments. The President explained earlier that you are considering various things. For bonding equipment, there was the announcement of collaboration with Nikon this time, and for cleaning equipment as well, I think there may be various opportunities going forward.

Do you believe you already have the elemental technologies and other factors you need as a company? If you could provide some hints again regarding the future direction of your strategic investments, I would appreciate it.

Regarding the next fiscal year, please explain your way of thinking in case the aforementioned JPY80 billion budget was not used up during this fiscal year. That is all.

Goto [A]: Since this is a strategic investment, we intend to strategically invest in various areas. I would first like you to understand that it is very difficult for us to share specific details with you as of today.

What we discussed specifically this time was the Nikon matter, and since we have used only about JPY3 billion for that, I understand that you are interested in what we will use the remainder for.

We are currently planning to use this investment in order to properly connect it to what comes next, so in that sense, including expansion in the wet cleaning area and other plus-alpha elements. After then, we would like to proceed with our next investments.

At this point, we intend to use it properly, so in that sense, we are not really assuming that we will not use it all, but if, for some reason, we were unable to use it all, that could happen. We will consider it at that time, but at present, we have the determination and plan to use it all.

As I mentioned earlier, when we have opportunities to share specific details with you, we would like to make announcements.

I understand it is somewhat frustrating that we cannot clearly tell you where and how at this time, but internally, we have been developing our long list and short list carefully over time, and we are working on it with the determination that we will do it for the future. If you could wait a little longer, I believe we will be able to disclose specific projects to you, so I would appreciate it if you could wait a little longer.

Nakamura [M]: Thank you.

Miura [M]: Mr. Nakanomyo, please.

Nakanomyo [Q]: I am Nakanomyo from Jefferies Securities. I have two questions.

My first question is related to the first question. I believe that CBA and the first generation of GAA are already emerging as businesses now. In these areas, is it the case that the level of technological requirements is increasing more than the increase in the number of process steps?

Takahashi [A]: Yes. We provided a roadmap of sales for future device transitions this time. We assume that the technological domains cultivated in Logic and the areas where we will develop technologies with a fairly high level of difficulty going forward can be where we can market our technological excellence as added value.

We assume that an increase in business volume is not simply due to an increase in the number of process steps, but largely due to other factors.

Nakanomyo [Q]: At present, has the phenomenon of sales price increases exceeding the number of process steps not occurred yet?

Takahashi [A]: We recognize that it is occurring little by little, but we assume it will become more pronounced going forward.

Nakanomyo [Q]: How should we view the depth of that? Is it something we can have a view on? I would like to know.

Takahashi [A]: It has been 50 years since we started doing business in wafer cleaning equipment, and our experience cultivated mainly in foundries is the foundation. We believe we have been able to provide customers with significant yield improvements and added value, including our technologies, the equipment itself, including the supply chain, and the overall level of completion, so if we can apply that in DRAM and NAND going forward, we assume that the likelihood is high.

Nakanomyo [Q]: Regarding slides 46 and 47, for the time being, I personally think NAND would be promising as business, but how scalable can it be? Were you able to capture PORs in peripheral processes such as scum cleaning?

Takahashi [A]: Yes. We have also obtained PORs from multiple customers, and we will proceed with brush-ups at those customers. We plan to sequentially apply and propose the technology to customers where we have not obtained it.

Nakanomyo [Q]: About how much business volume can be expected for back-side cleaning?

Takahashi [A]: This area, as we also talked about EUV this time, at present we recognize it will account for about 20% to 30% of the overall volume.

Nakanomyo [Q]: What did you mean by "20% to 30%"?

Takahashi [A]: It is difficult to define, but we think the volume of investments by leading-edge customers is around 20% to 30%.

Nakanomyo [Q]: In terms of sales, simply put, about how much business volume would that be?

Takahashi [A]: Since it depends on the future market situation, I think it is difficult to convert it into our figures. We would appreciate it if you could have an image of it as a ratio.

Nakanomyo [Q]: On page 49, regarding this exponential word line discussion, is this at the evaluation stage?

Takahashi [A]: We assume this will come out going forward, and it is probably still at a pre-evaluation stage.

Nakanomyo [Q]: In that sense, your company is fairly differentiated.

Takahashi [A]: Yes. We are very confident.

Nakanomyo [M]: Thank you. That is all.

Moderator [M]: Thank you, Mr. Nakanomyo. Mr. Wadaki, please.

Wadaki [Q]: I am Wadaki from Morgan Stanley MUFG Securities. First, compared with the IR Day sessions in the past, I feel you have presented a very positive outlook for the future. Up to now, in a sense, wet cleaning has had a rather tough growth outlook for the future compared with others, and in terms of strategy, you have shown growth stories here. Has there been something like securing a clearer outlook for TAM for cleaning as a result of various technological initiatives?

Mikawa [A]: I am Mikawa, in charge of this technology strategy. Regarding your question, we are working in collaboration with places like Imec (imec) and IBM to anticipate technology. Based on the process flows shown there, we are anticipating in advance new process steps in areas like these.

In addition, not only anticipating, but also while advancing PoC verification-level work, as a strategy based on various internal discussions on the point that we may be able to enter these processes, the content shown at this IR Day is that we believe we can target areas like these.

Wadaki [Q]: My impression is that, over the past year or so, whether it is BSPDN or CBA, when actually made performance turned out to be very well, and there is talk of applying them across the industry all at once. And since bonding is important in these, I felt that the outlook became very positive all of a sudden, but is it what is actually happening now?

Mikawa [A]: Yes, indeed. We have strengths in the FEOL area, while we had difficulty entering the BEOL area. Now, there is a shift of the front-side processes to the backside, and a new phase has started. Alternatively, as with 3D, there has come to be a greater need for cleaning at so-called steps, and since our strengths in FEOL cleaning can be leveraged in a new way. So we can say that the phase has shifted, and opportunities for us have increased.

Another point is that device structures have become 3D, and lateral etching has become very process-specific.

This part was also asked about earlier, and it is an area where we can strongly demonstrate our strengths in wet processes using chemicals. Meanwhile, the competitors are likely to leverage dry etching, rather than compete in wet cleaning. If we establish a solution and can win POR, we believe it can be sufficiently reflected in equipment unit prices as well.

Wadaki [Q]: Thank you. There is another question—it is said that around the second half of next year will be a big year. Could you tell us, within the scope of what you can say, the likelihood of this, what kind of peak it is likely to be, and your company's response?

Okamoto [A]: I am Okamoto. Thank you for your question. Our current feeling is that it will likely be a year that exceeds the 2024 level.

Wadaki [Q]: Are preparations underway?

Okamoto [A]: Last time, when the demand rose very sharply, we had various difficulties accommodating it, so since then, the capacity and the facilities have been increased under the leadership of Mr. Goto. Within that, we are improving productivity, and we are also strengthening the supply chain, so we believe there is no concern.

Wadaki [M]: Thank you very much.

Moderator [M]: Thank you, Mr. Wadaki. Then, we would like to make the next one the final question.

Mr. Yoshida, please.

Yoshida [Q]: Thank you. First, I would like to ask Mr. Takahashi, could you explain the background as to why, for NAND exponential word line contact, it will rely on single-wafer cleaning rather than batch cleaning?

In addition, with this method, while I think the number of etching processes will decrease, but on the other hand, the lithography processes would increase and costs would rise. How about that?

Takahashi [A]: Thank you. Each time, etching requires stripping the resist, and we think it may be difficult to control that with batch processing. In terms of within-wafer uniformity, particularly as processing times become shorter, single-wafer processing becomes more advantageous.

For example, if over-processing occurs, there is also a concern that the shape of the holes that were etched with effort may change slightly during the wet process, so we assume that single-wafer processing, which makes such control easier, will be favored.

The other point is total cost. I think it depends on how much lithography will be required. There are still some areas we have not yet factored in the overall cost balance, or what it will look like before and after. We would like to examine, going forward, how much benefit there is when the three processes shown earlier are repeated, not limited to wet processing. Based on that, we think we can reconsider the added value of cleaning.

Yoshida [Q]: Thank you. I would like to ask Nishimura, on direct imaging. I believe LeVina for PLP is for interposers, but what are your advantages over competing direct imaging exposure tools? In addition, recently, I think other technologies have been emerging, such as digital exposure and nanoimprint. Compared with those, what are the advantages of LeVina?

Nishimura [A]: As I explained earlier, this GLV is unique to SCREEN, and other manufacturers use devices such as DMD. For GLV, 8,000-something ribbons move and imprint patterns, so that it can be finished with very high precision.

First, in that regard, we believe that SCREEN is differentiated in terms of forming RDL with precision.

Yoshida [Q]: Compared with photolithography and nanoimprint, is it something your direct imaging equipment can handle on ultra-large substrates?

Nishimura [A]: At the level of 2 microns by 2 microns, we can sufficiently handle. However, for stricter requirements, such as 1 micron or somewhat narrower line widths, I think development going forward will be necessary.

Moderator [M]: Thank you, Mr. Yoshida.

This concludes today's IR Day event.

With that, we will conclude SCREEN Group IR Day 2025. Thank you very much for joining us today despite your busy schedules.

[END]

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